

ZZZ1

PCB
Part Number = DA6001SK01B
LA-F902P

PCB@

Compal Confidential

Schematics Document

AMD AM4 Platform

DGPU AMD R17M-1-70

LA-F902P REV: 1.0
2018-03-22

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Issued Date	2015/01/23	Deciphered Date	2017/01/23	Title	
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Voltage Rails	Description	S0	S3	S5
Power Plane				
+DC20V	Adapter power supply (20V)	ON	ON	ON
+APU_CORE	Core voltage for processor core current	ON	OFF	OFF
+APU_CORE_NB	Voltage for processor Northbridge (NB) current	ON	OFF	OFF
+APU_CORE_FCH	Voltage for processor VDDCR_FCH	ON	ON	ON
+0.95_1.05VALW	0.95V always on power rail	ON	ON	ON
+0.95_1.05VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.2V_VDDQ	VDDQ power rail for APU and DDR	ON	ON	OFF
+0.6VS_VTT	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VL_RTC	3.3V RTC power	ON	ON	ON
+RTC_APU	1.5V RTC power	ON	ON	ON
+3V3_DSW	3.3V always for EC only	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+0.775VALW	0.775V always on power rail	ON	ON	ON
+VGA_CORE_S0	VGA power	ON	OFF	OFF
+1.35V_VRM	1.35V VGA/VRAM power	ON	OFF	OFF
+3VGS	3.3V VGA power	ON	OFF	OFF
+1.8VGS	1.8V VGA power	ON	OFF	OFF
+0.95VGS	0.95V VGA power	ON	OFF	OFF

Port	Device
0	LAN
1	WLAN
2	multi Function
3	

Port	Device
0	HDD
1	ODD

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Port	Device
0	USB20- (HUB1)
1	USB20- (HUB2)
2	USB30(2.0)- (Rear I/O)
3	USB30(2.0)- (Side I/O)
0	
1	
2	USB30- (Rear I/O)
3	USB30- (Side I/O)

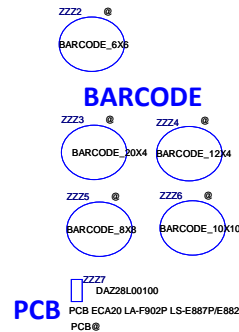
Port	Device
0	JUSB1
1	JUSB2
2	JUSB3
3	Card Reader

Port	Device
0	WLAN
1	N/A
2	Touch Panel
3	Camera

BOM Structure	BTO Item
@	Unpop
DIS@	DIS pop component
UMA@	UMA pop component
EMI@	EMI pop component
@EMI@	EMI unpop component
ESD@	ESD pop component
@ESD@	ESD unpop component
DIS_EMI@	EMI pop component for DIS SKU
@RF@	RF unpop component
BR@	Component for Bristol CPU
RAV@	Component for RAVEN CPU
CVT@	eDP to LVDS Converter IC
SC@	Scalar + HDMIIN
HDMIIN@	pop componet for HDMIIN
EMI_HDMIIN@	EMI pop componet for HDMIIN
ESD_HDMIIN@	ESD pop componet for HDMIIN
TPM@	Hardware TPM SKU Componet
STPM@	Software TPM SKU Componet
TPMB@	TPM SKU for Bristol CPU
TPMR@	TPM SKU for Raven CPU
SMART@	For SMART POWER ON
NSMART@	Non-SMART Power ON
AMP@	Normal AMP
DSP@	Smart AMP
DSP_EMI@	EMI solution for Smart AMP
IRCAM@	IR CAMERA
AMP_EMI@	EMI solution for Normal AMP

Device	Address	HEX	Device	Address	HEX
SB-TSI (APU)	1001 - 100xb	98H	RTD2506S	1001 - 010xb	94H
DGPU Temp.	1000 - 001xb	82H	CONVERTOR	0110 - 001xb	62H
Thermal IC	1001 - 101xb	9AH	Smart AMP	1001 - 101xb	9AH
RTD2136N-CGT	1001 - 010xb	94H	RTC IC	1010 - 001xb	A2H

Device	Address	HEX
DDR JDIMM1	1010 - 000xb	A0H
DDR JDIMM2	1010 - 010xb	A4H
RTD2506S	1001 - 010xb	94H



SKU ID(Project) Table

SKU	BOM Configure Table
EVT (MB1)	451AAR38L01: UMA@/BR@/SC@/HDMIIN@/IRCAM@/NSMART@/AMP@/STPM@/PCB@ X4EAAR38L01: EMI@/ESD@/EMI_HDMIIN@/ESD_HDMIIN@/AMP_EMI@
EVT (MB2)	451AAR38L02: DIS@/BR@/SC@/HDMIIN@/IRCAM@/NSMART@/AMP@/STPM@/PCB@ X4EAAR38L02: EMI@/ESD@/DIS_EMI@/EMI_HDMIIN@/ESD_HDMIIN@/AMP_EMI@
EVT (MB3)	451AAR38L03: DIS@/BR@/SC@/HDMIIN@/IRCAM@/SMART@/AMP@/STPM@/PCB@ X4EAAR38L02: EMI@/ESD@/DIS_EMI@/EMI_HDMIIN@/ESD_HDMIIN@/AMP_EMI@
EVT (MB4)	451AAR38L03: DIS@/BR@/SC@/HDMIIN@/IRCAM@/SMART@/DSP@/TPM@/TPMB@/PCB@ X4EAAR38L03: EMI@/ESD@/DIS_EMI@/EMI_HDMIIN@/ESD_HDMIIN@/DSP_EMI@

X7676338L01 ALT. GROUP PARTS 2G SAMSUNG EOS10
X7676338L02 ALT. GROUP PARTS 2G HYNIX EOS10
X7676338L03 ALT. GROUP PARTS 2G MICRON EOS10

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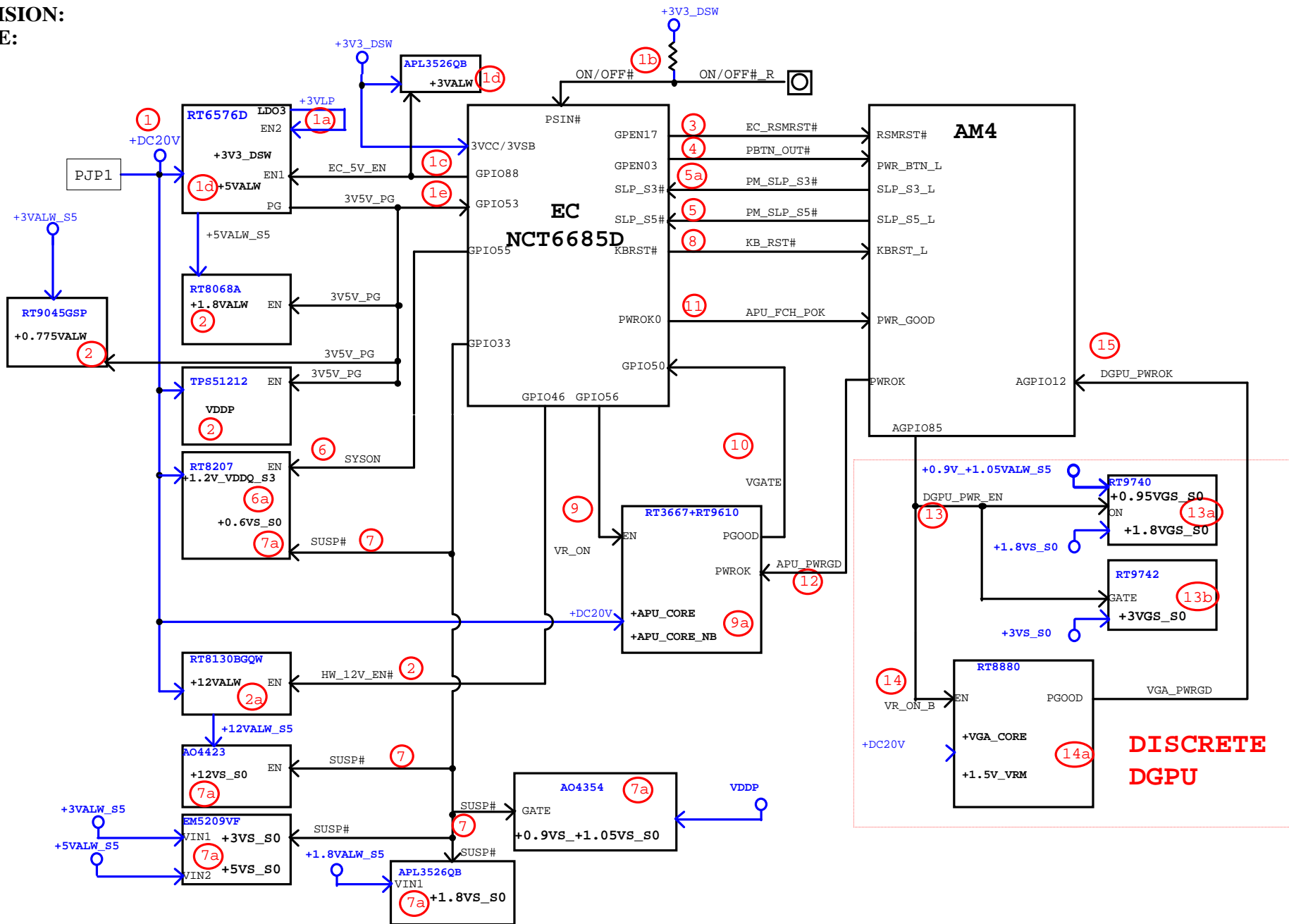
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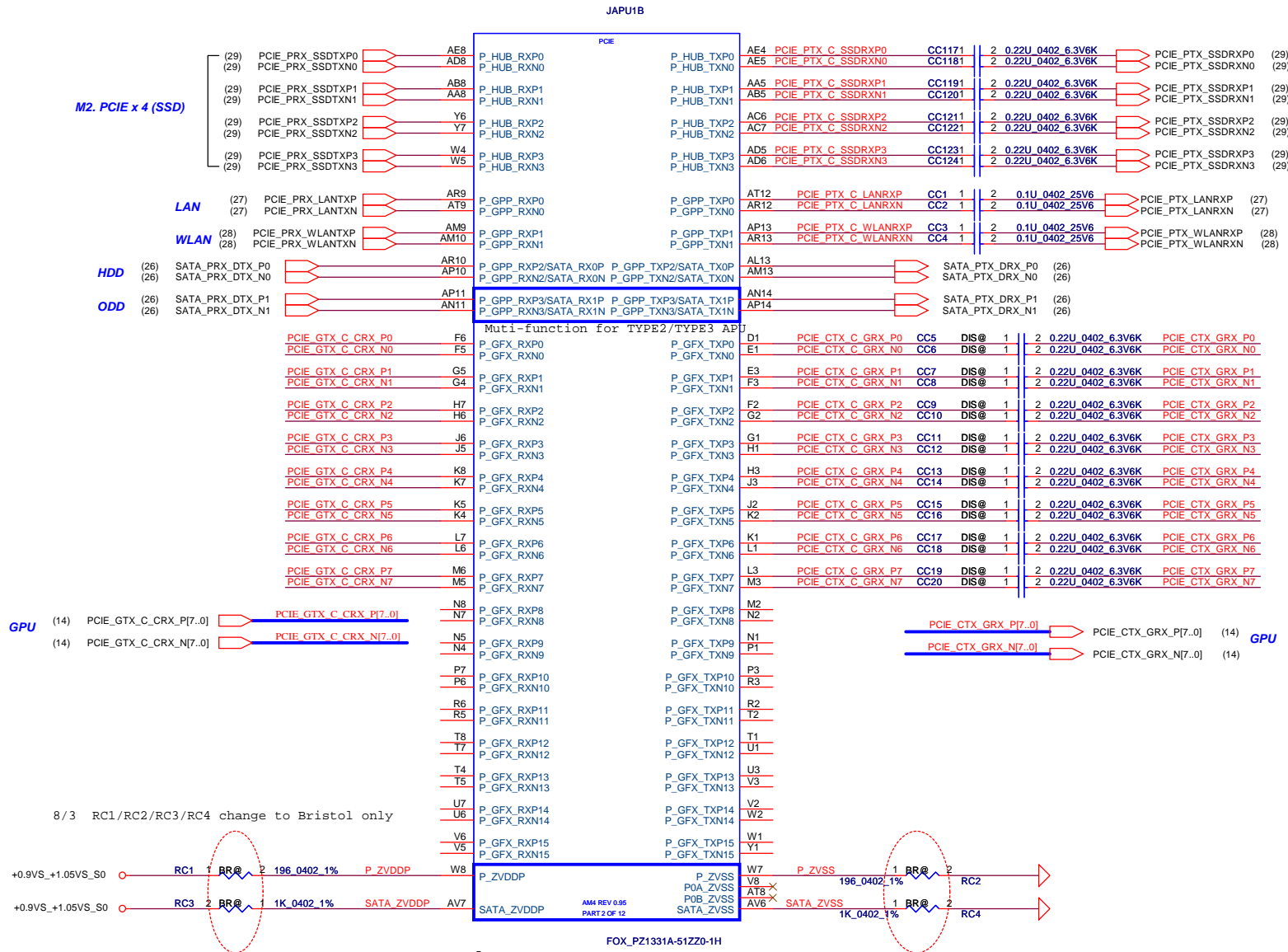
Platform Power Sequence

PCB NAME:

REVISION:

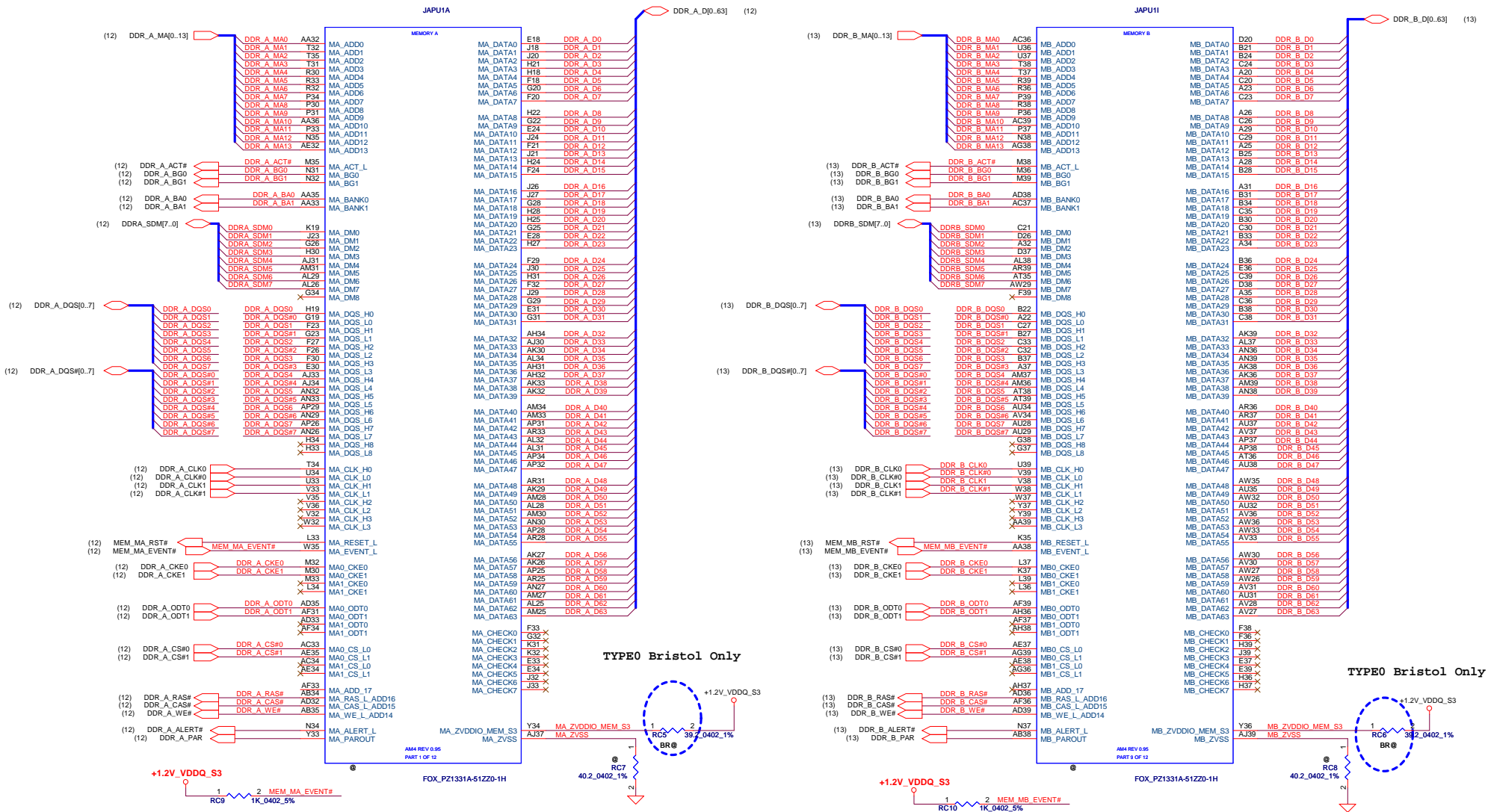
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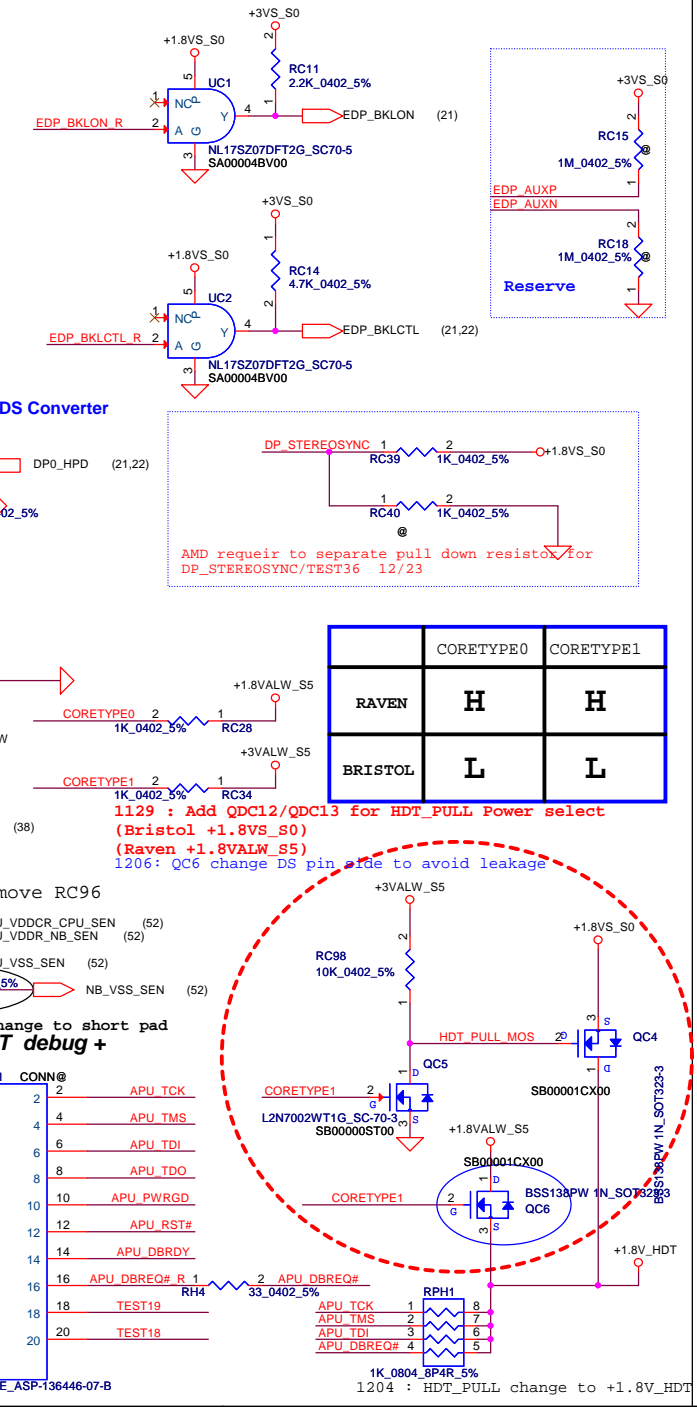
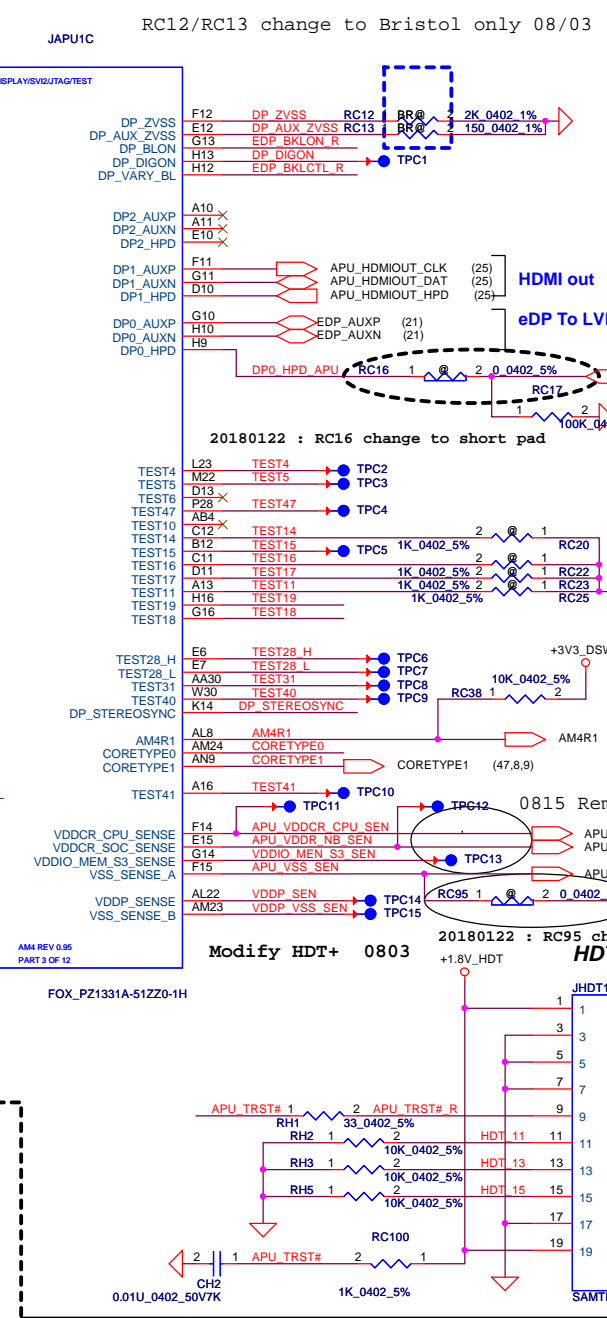
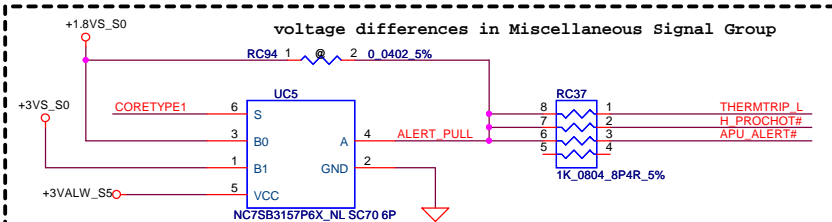


P_ZVDDP / P_ZVSS AM4 TYPE0 only (Bristol)
SATA_ZVDDP / SATA_ZVSS AM4 TYPE0 only (Bristol)
POA_ZVSS / POB_ZVSS AM4 TYPE2 only (Summit Ridge)

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Size		Document Number		Rev	
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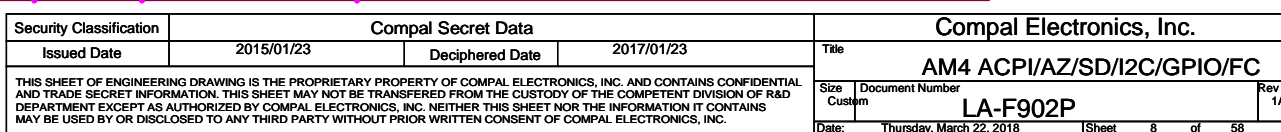
HDMI-OUT LANE Mapping	
DP PORT	HDMI-OUT
DP1_TXP/N0	HDMI_TX2+-
DP1_TXP/N1	HDMI_TX1+-
DP1_TXP/N2	HDMI_TX0+-
DP1_TXP/N3	HDMI_CLK+-
DP1_AUXP	DDC_CLK
DP1_AUXN	DDC_DATA



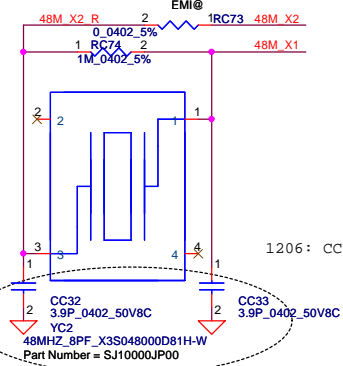
	CORETYPE0	CORETYPE1
RAVEN	H	H
BRISTOL	L	L

```
1129 : Add QDC12/QDC13 for HDT_PULL Power select
(Bristol +1.8VS_S0)
(Raven +1.8VALW_S5)
1206: QC6 change DS pin side to avoid leakage
```

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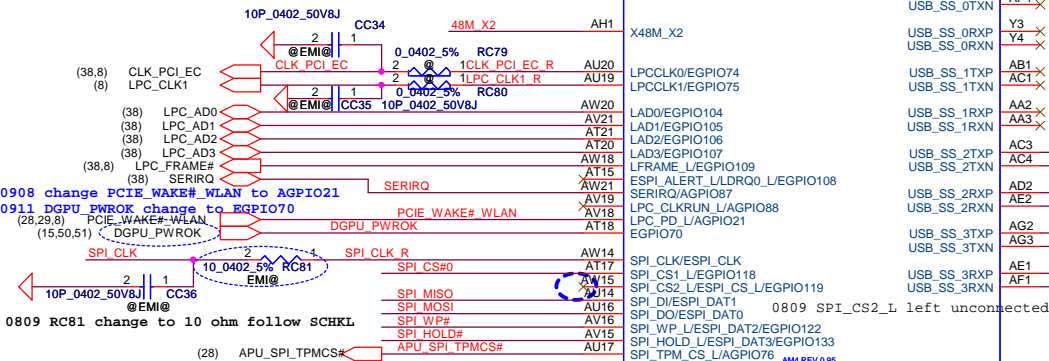


48MHz CRYSTAL



1206: CC32/CC33 change to 3.9P

VGA
LAN
WLAN
SSD

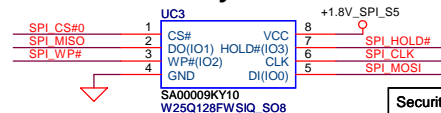


1206: reserve 0 ohm from +1.8VS_S0

0809 SPI_DI pull-high only for SPI_TPM

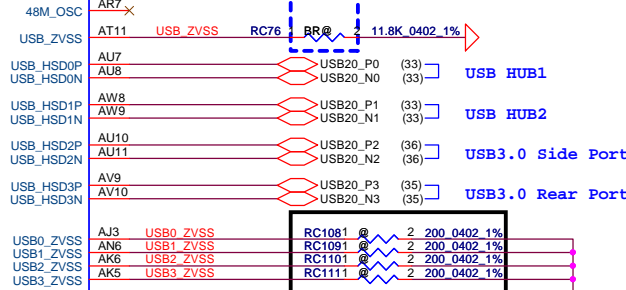
(28) SPI_MISO
(28) SPI_CLK
(28) SPI_MOSI

BIOS ROM
SPI ROM 16MByte/1.8V



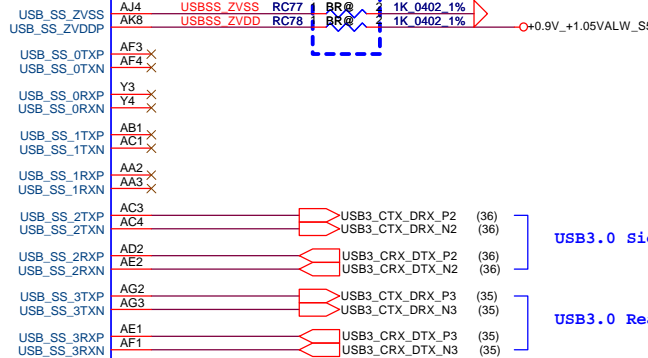
JAPU1E

CLK/USB/SPI/PC



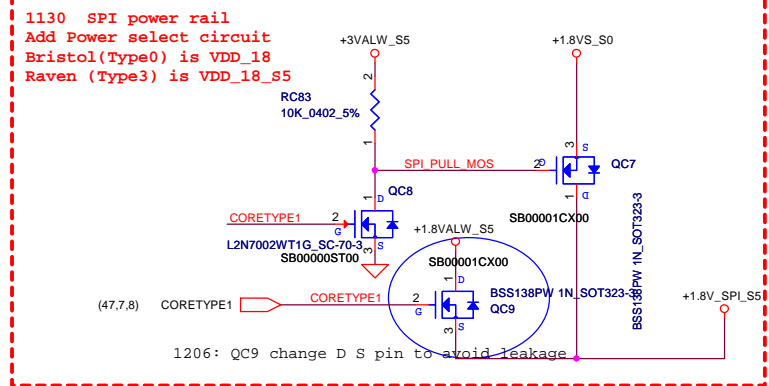
0816 Reserve RC108~111 for USB0_ZVSS~USB3_ZVSS
RC76/RC77/RC78 change to Bristol only 08/03

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USB3.0 Side Port (Gen1)

USB3.0 Rear Port (Gen2)

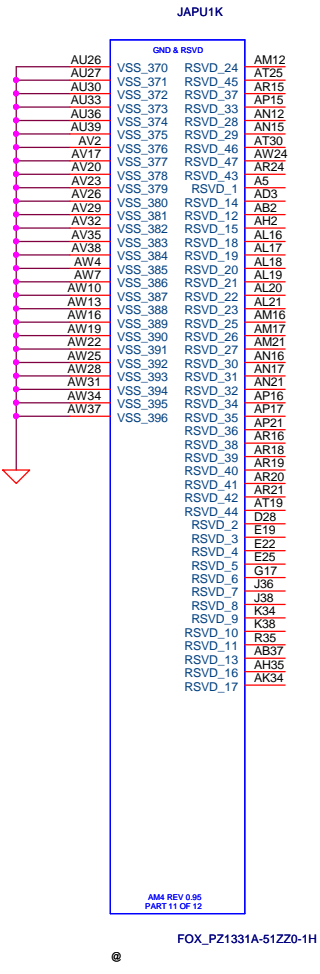
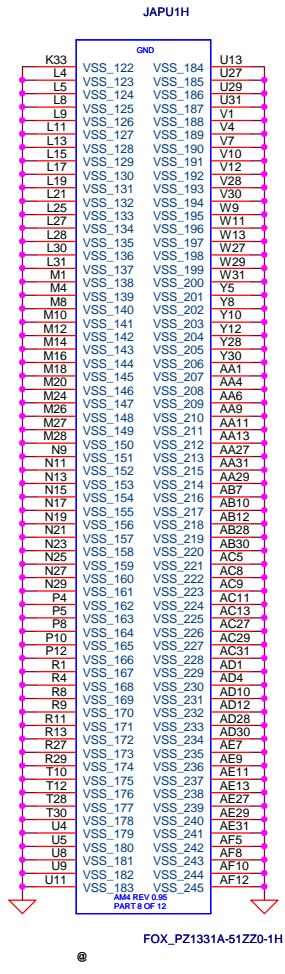
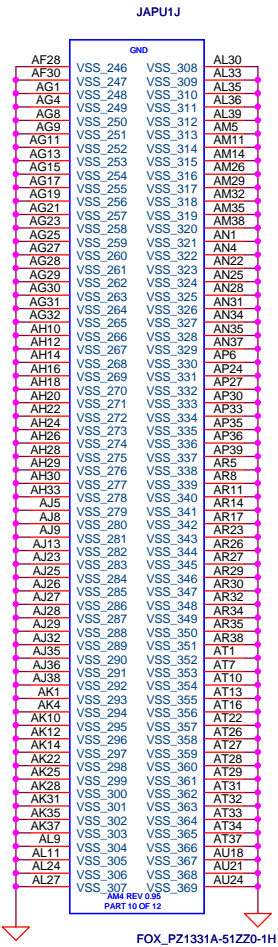
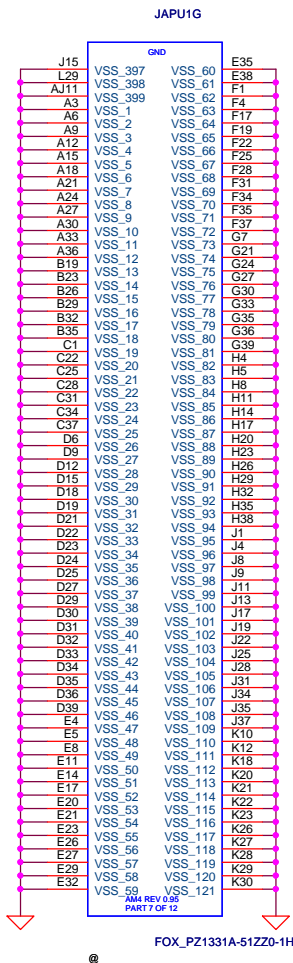


1130 SPI power rail
Add Power select circuit
Bristol(Type0) is VDD_18
Raven (Type3) is VDD_18_S5

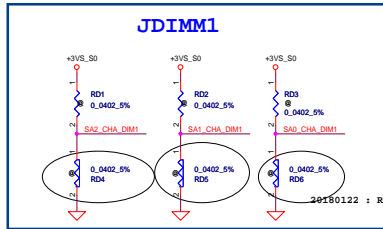
1206: Q9C change D S pin to avoid leakage

20180118
Remove SPI ROM socket
Co-layout

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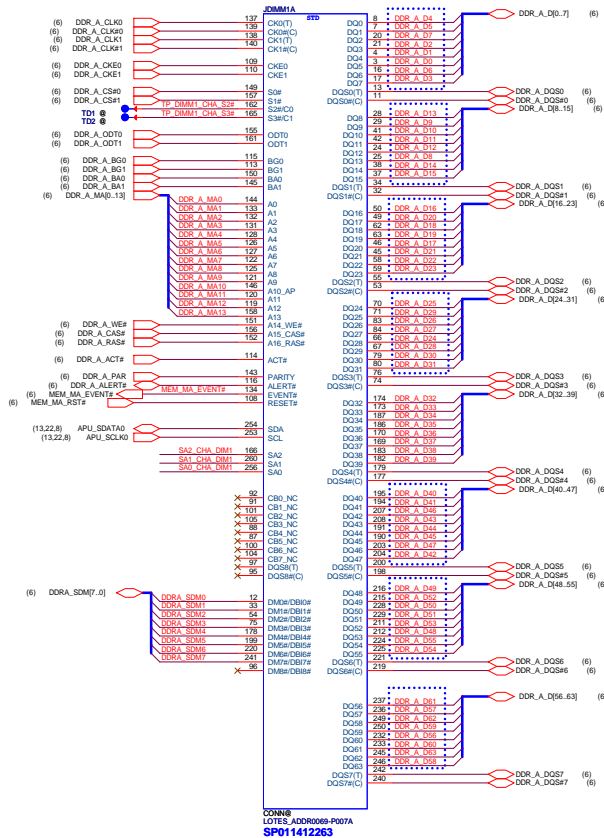
CHANNEL-A



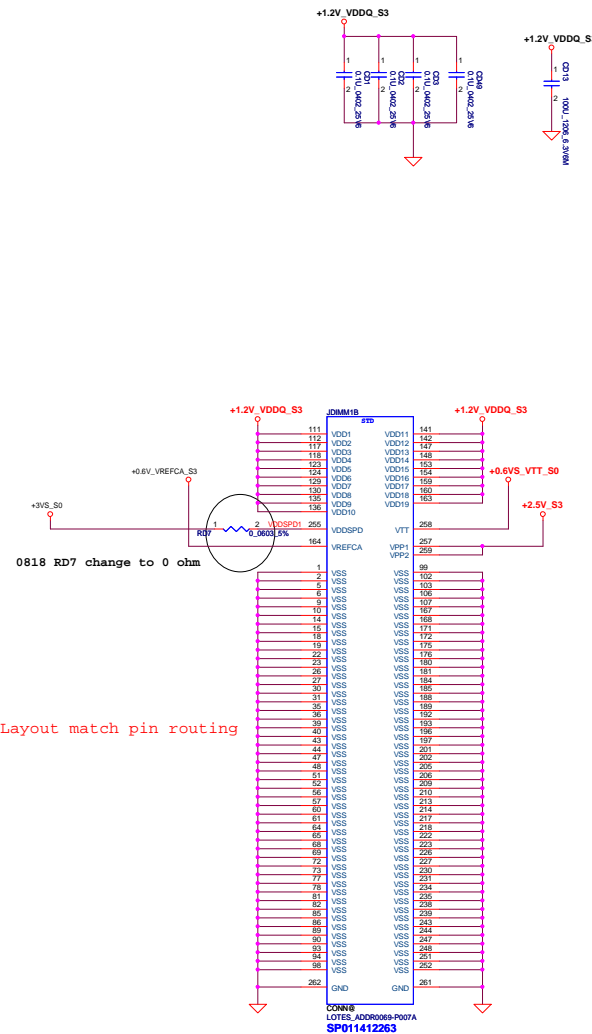
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
 WRITE ADDRESS: 0xA0
 READ ADDRESS: 0xA1
 SA0 = 0; SA1 = 0; SA2 = 0.

(8.0 mm) STD



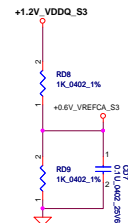
CONN6
 LOTES_ADDR0069-P007A
 SP011412263



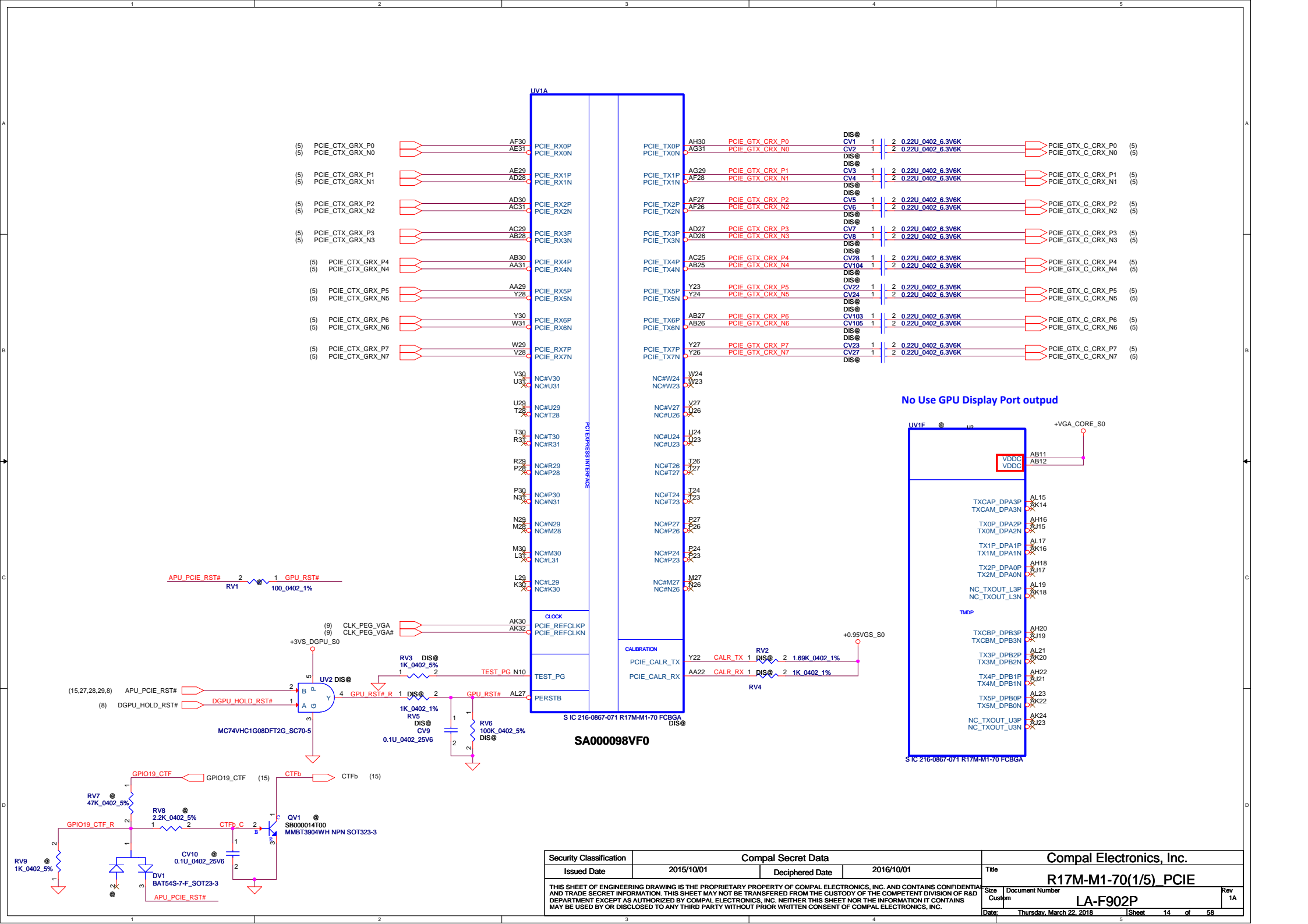
Layout Note:
 PLACE THE CAP WITHIN 200 MILS
 FROM THE JDIMM1

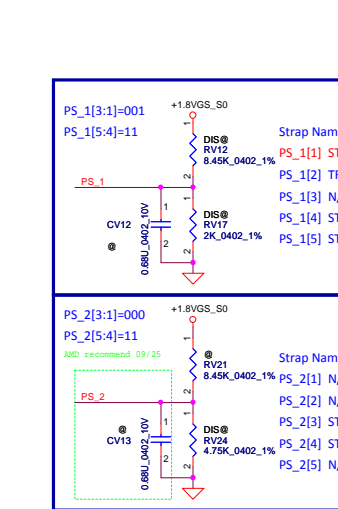
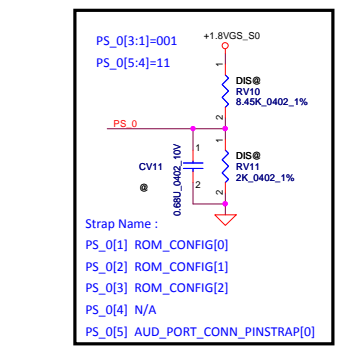
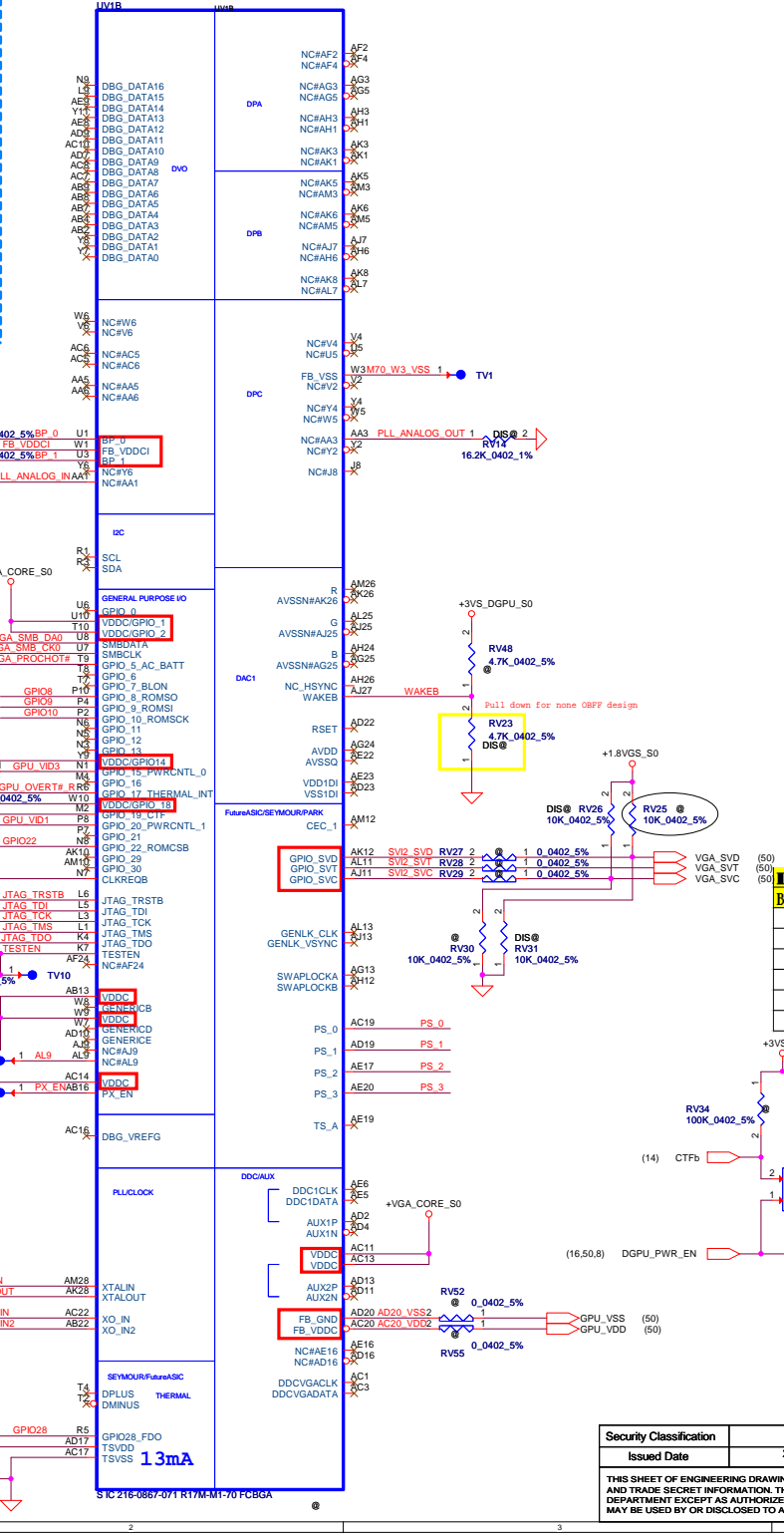
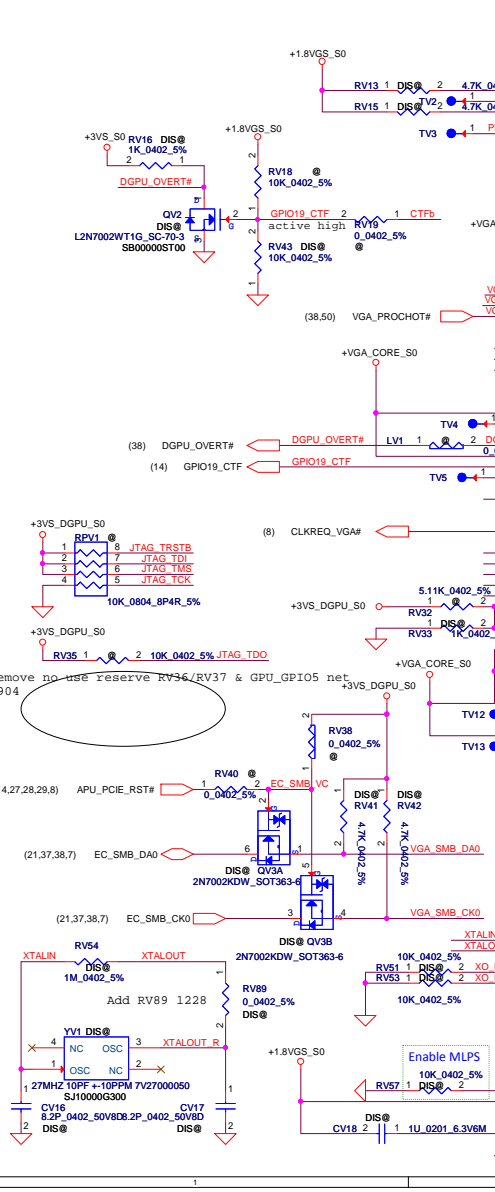
Layout Note:
 Place near JDIMM1

Layout Note:
 Place near JDIMM1



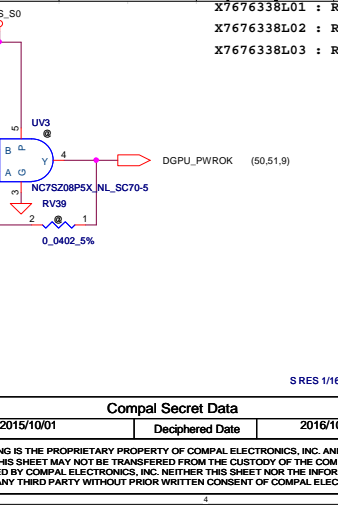
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[illegible]

Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

LPS MEMORY ID Setting:						
Board Config[2:0]		Memory Type	Configuration	Channel Size	Vendor P/N	Compal P/N
ID	[2:0]					
0	000	Samsung gDDR5	128Mx32 2PCS	1GB	K4G41325FE-HC28	SA00009TT400
1	001	Hynix gDDR5	128Mx32 2PCS	1GB	H5GC4H24ATR-T2C	SA00008HQ00
2	010	Micron gDDR5	256Mx32 2PCS	2GB	MT51TJ256M32HF-70:A	SA00009TV00
3	011	Samsung gDDR5	256Mx32 2PCS	2GB	K4G803252FE-HC28	SA00009ZD10
4	100	Hynix gDDR5	256Mx32 2PCS	2GB	H5GC8H24ATR-ROC	SA00009JL00



RV20 = 4.53K , RV22 = 4.99K (SAMSUNG 2G)
 RV20 = 4.53K , RV22 = 4.99K (HYNIX 2G)
 RV20 = 4.53K , RV22 = 2K (MICRON 2G)

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
 PS_3[1] BOARD_CONFIG[0] (Memory ID)
 PS_3[2] BOARD_CONFIG[1] (Memory ID)
 PS_3[3] BOARD_CONFIG[2] (Memory ID)
 PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
 PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

RV20 X76_M2@ RV22 X76_M2@

SD034453180
SW 4.53K +1% 0402

RV20 X76_H2@ RV22 X76_H2@

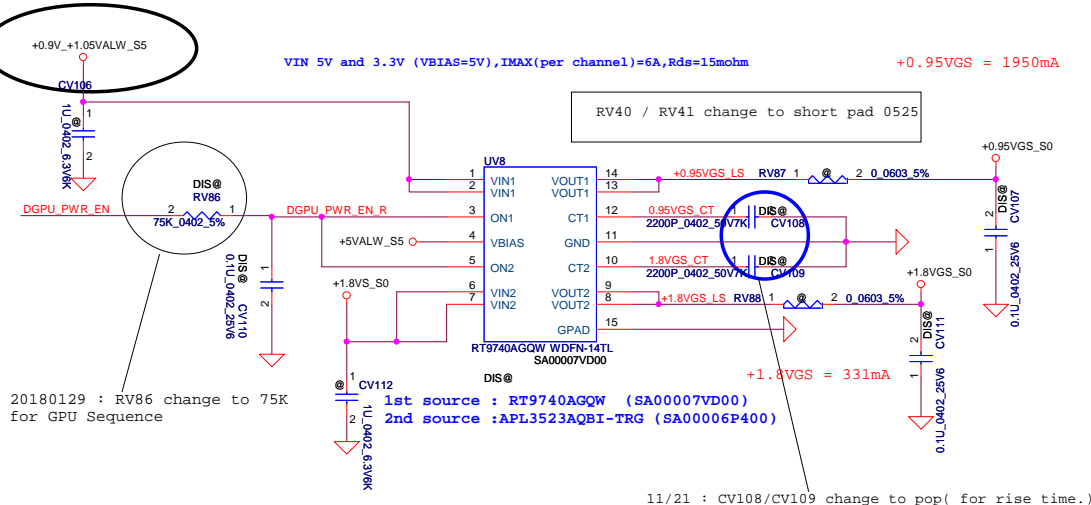
SD034453180
S RES 1/16W 2K +5% 0402

RV20 X76_H2@ RV22 X76_H2@

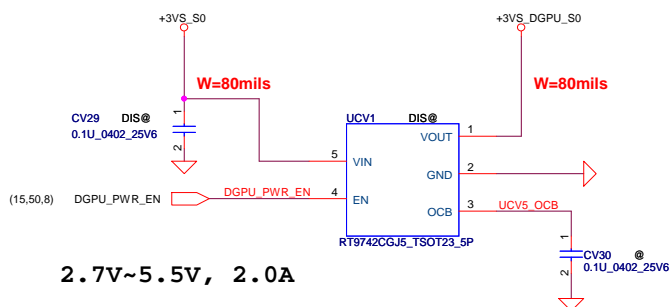
SD034499180
S RES 1/16W 4.53K +1% 0402

+1.8VS TO +1.8VGS
+0.95VS TO +0.95VGS
Load switch

Change +0.95VGS source to +0.95V_+1.05VALW_S5 0804

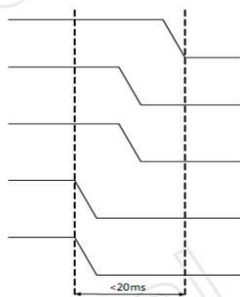
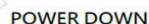
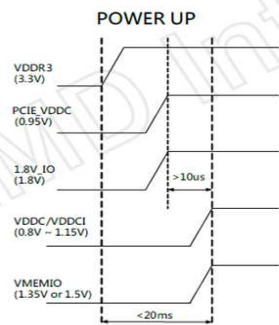


+3VS to +3VGS



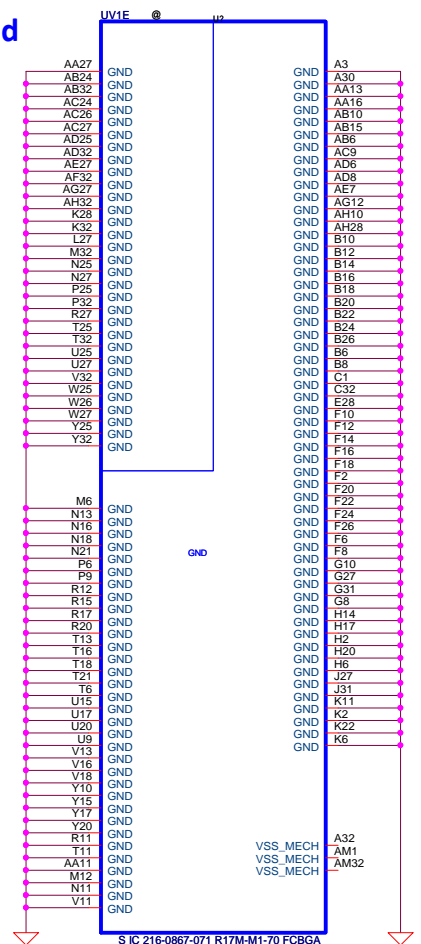
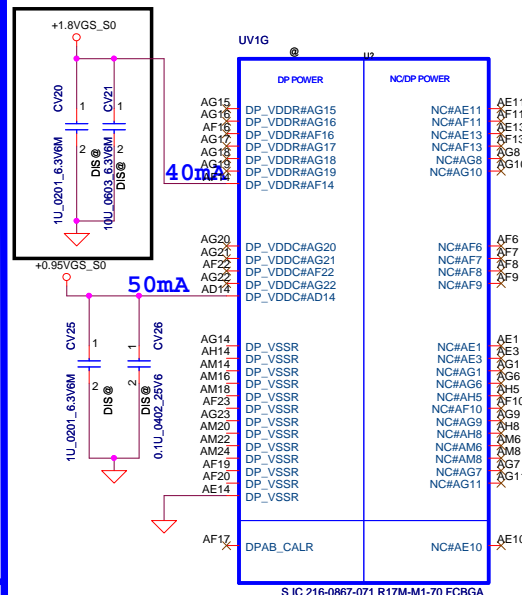
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

- 1.the 3.3-V rail ramp up first.
- 2.the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up



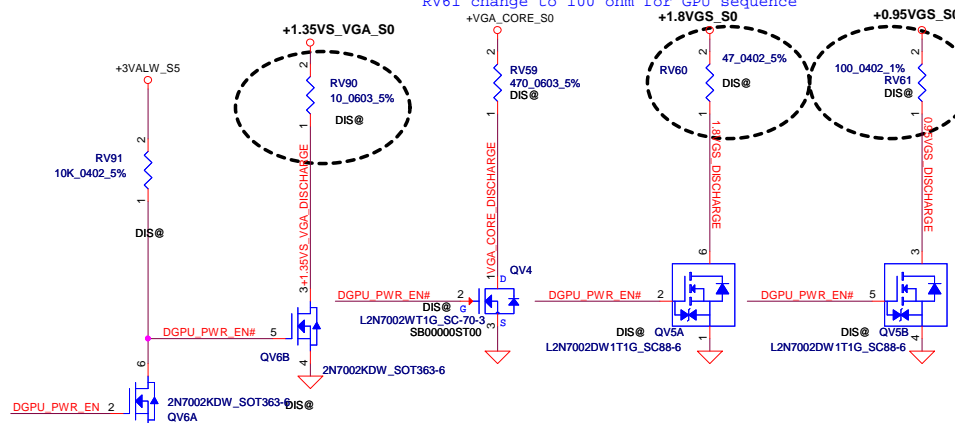
No Use GPU Display Port output

```
0804 follow DG modify Caps
Remove CV19
```

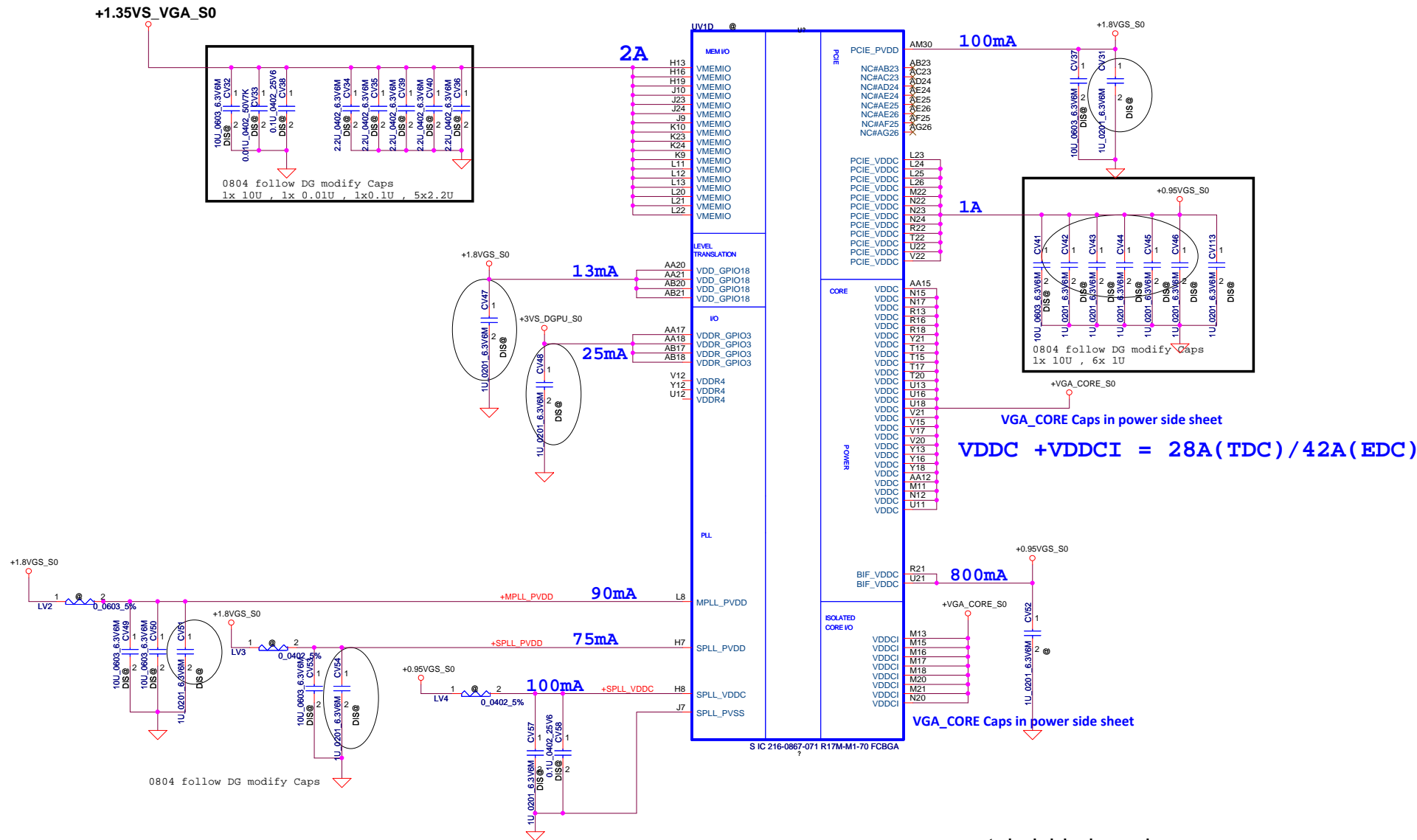


1130: RV90 change to 10 ohm (improve discharge)

20180129 : RV60 change to 47 ohm for GPU Sequence
RV61 change to 100 ohm for GPU sequence



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Issued Date	2015/10/01	Deciphered Date	2016/10/01	Title	R17M-M1-70 (3/5) PWR/GND
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				Custom	1.
Date: Thursday, March 22, 2018				Sheet	16 of 58



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Issued Date	2015/10/01	Deciphered Date	2016/10/01	Title	R17M-M1-70(4/5) PWR
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				Document Number	LA-E883P M/B
				Date	Thursday, March 22, 2018
				Sheet	17 of 58
				Rev	1A

SA00009TV30

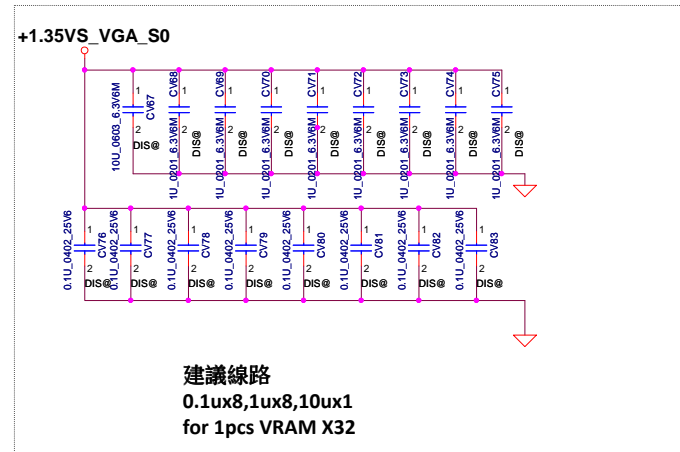
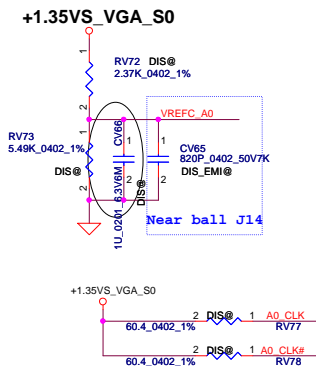
X76_M2@

UV4

SA00009U120

X76_H2@

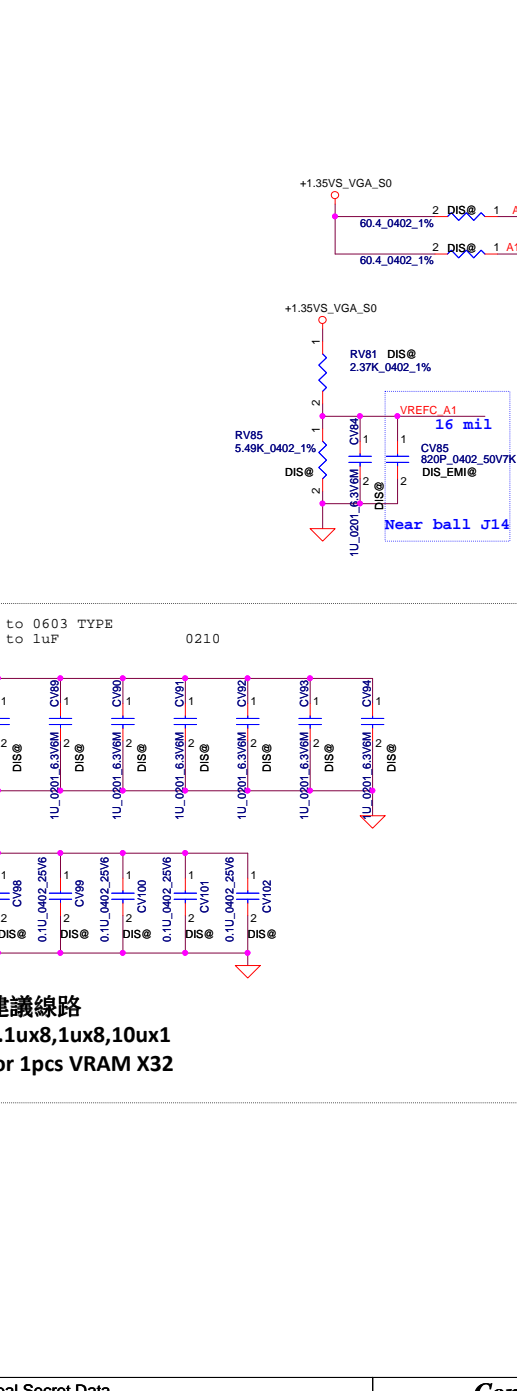
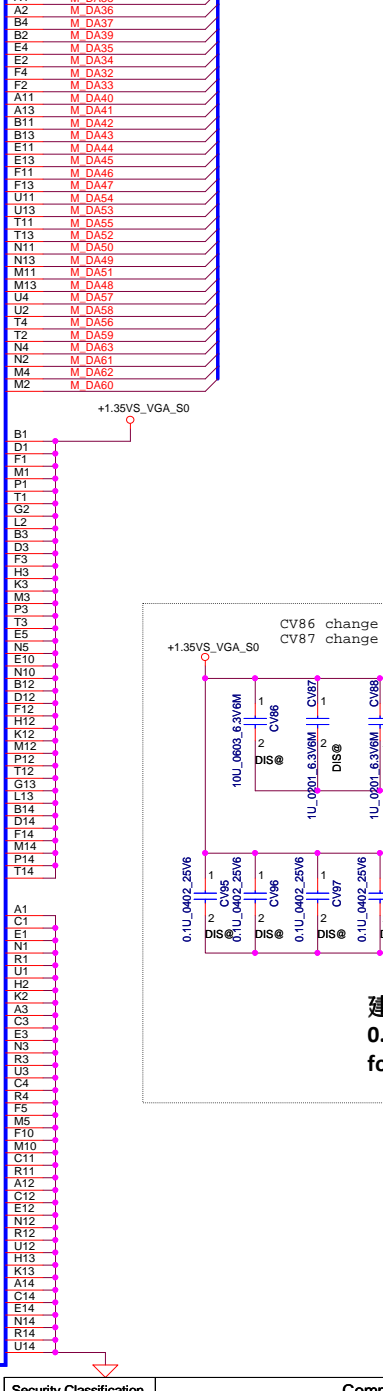
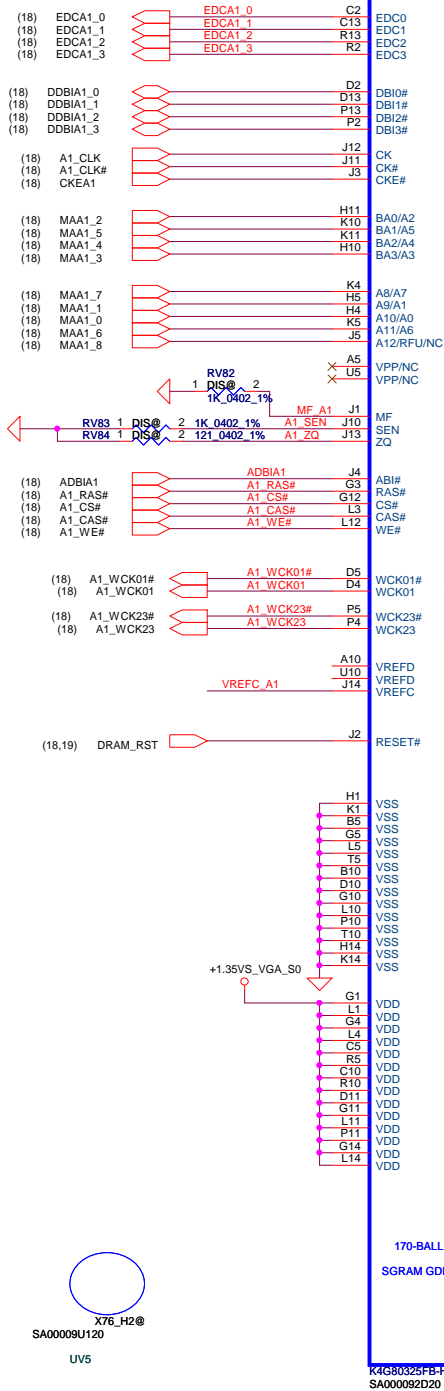
UV4



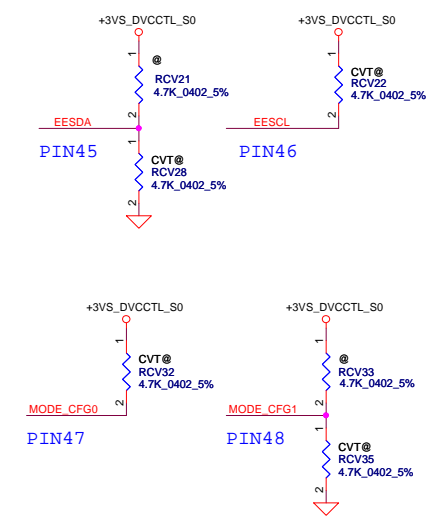
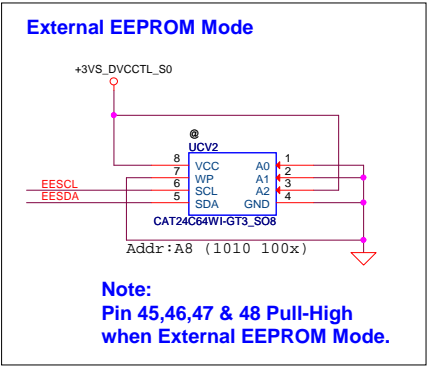
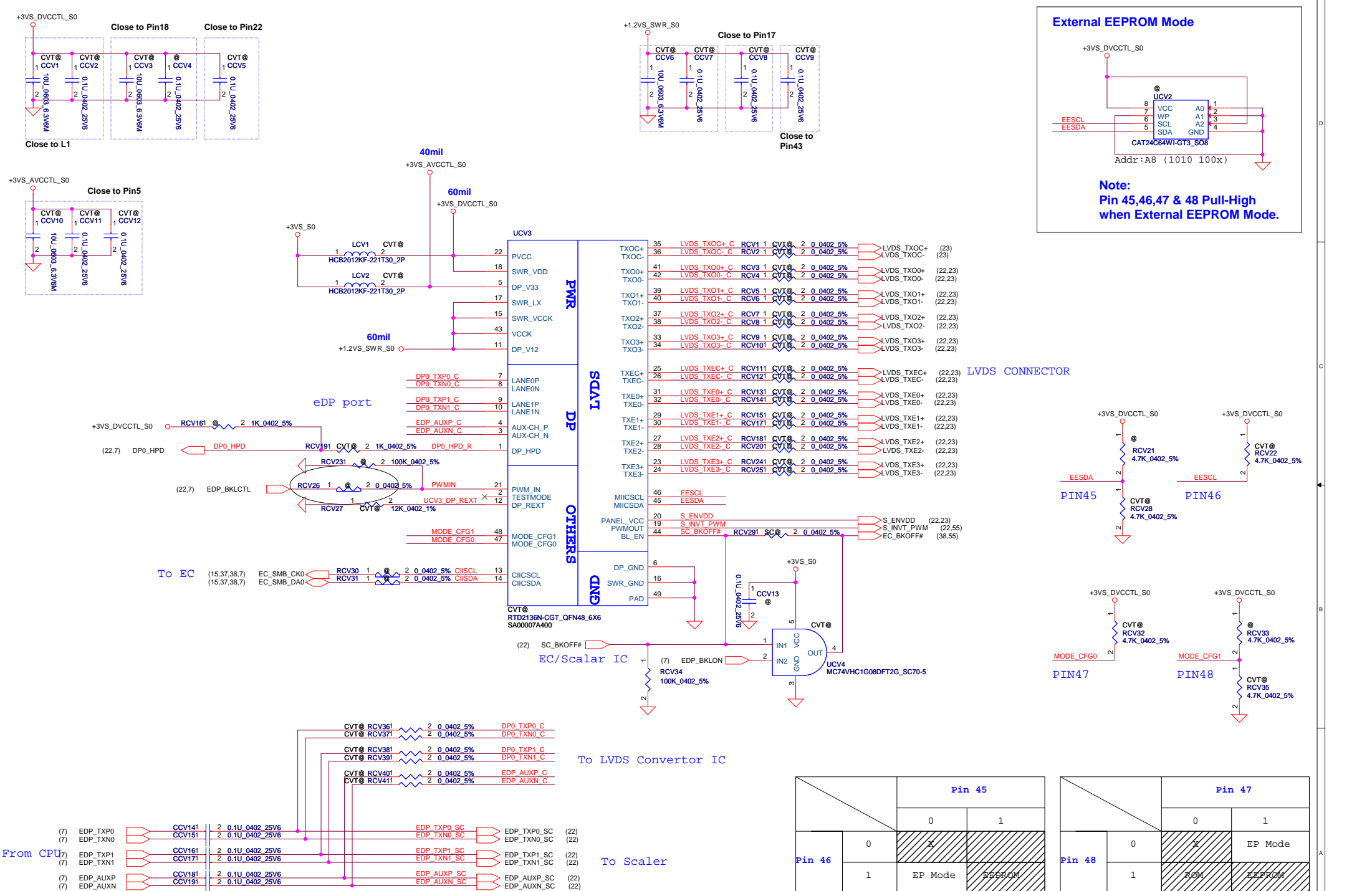
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2013/03/01	Deciphered Date	2014/03/01	Title	GDDR5 VRAM A Lower	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev 1A
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				Date:	Thursday, March 22, 2018	Sheet 19 of 56

Memory Partition A Upper

- 32 bits

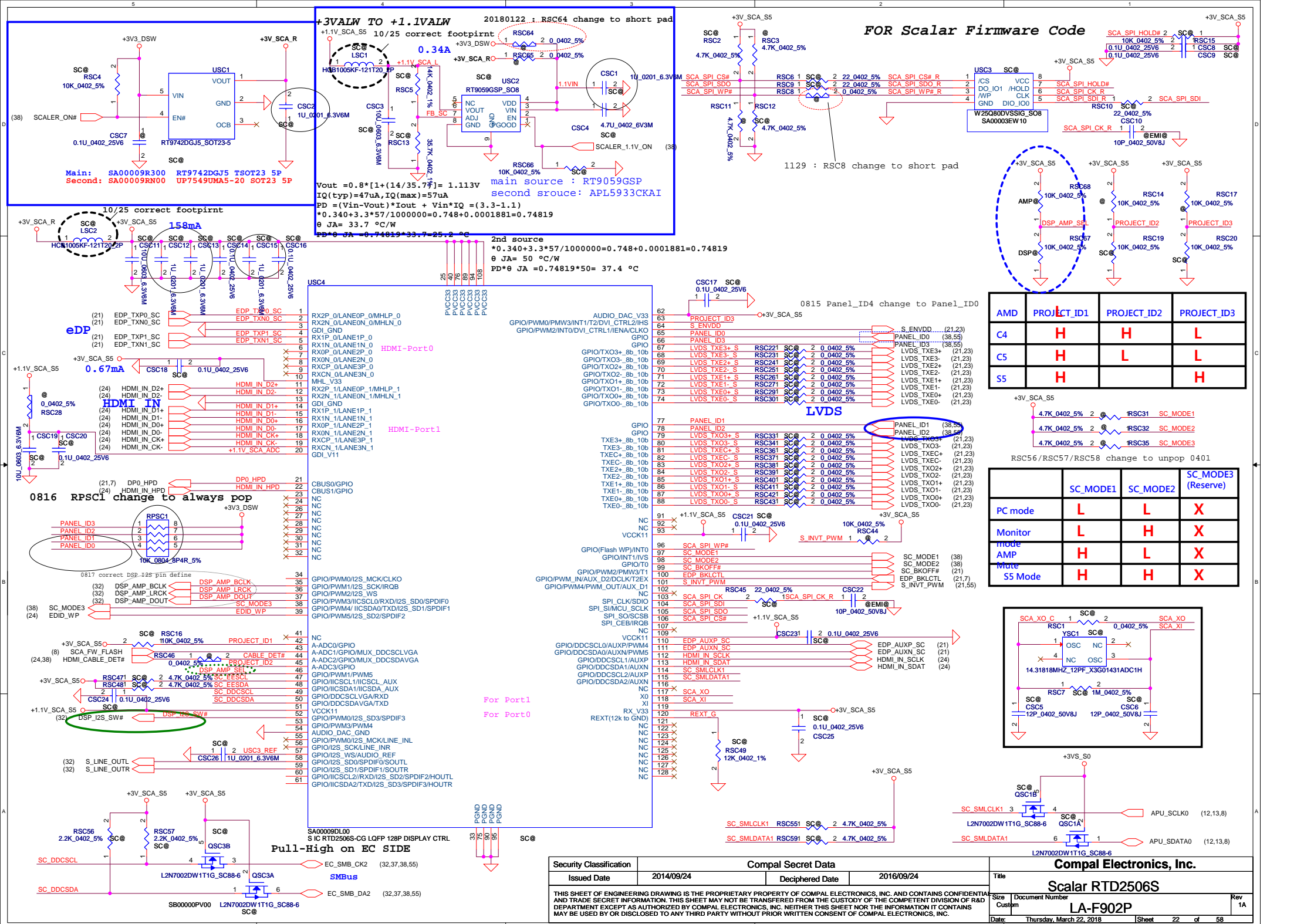


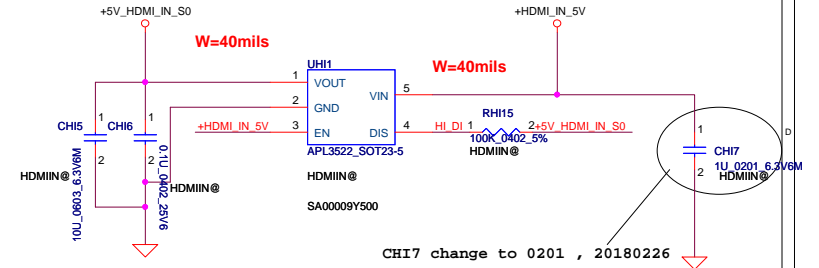
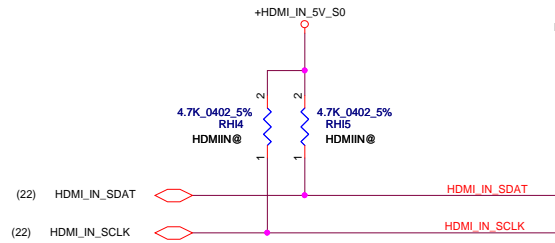
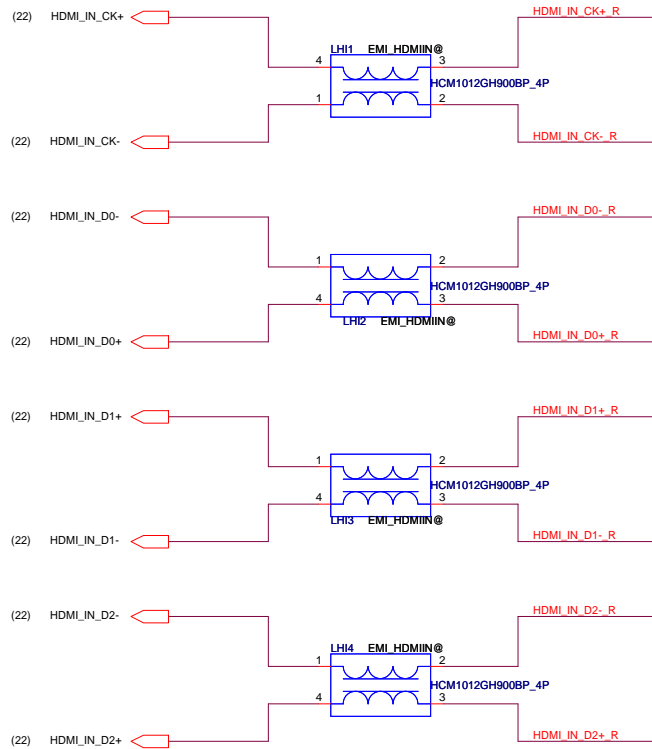
Security Classification		Compal Secret Data		Title	
Issued Date	2013/03/01	Deciphered Date	2014/03/01	GDDR5 A Upper	
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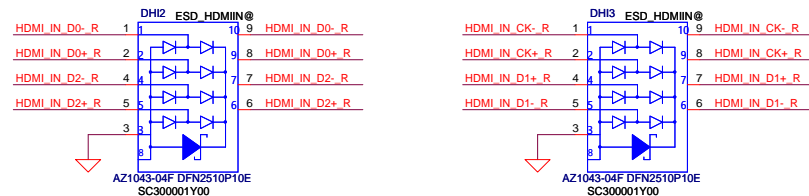
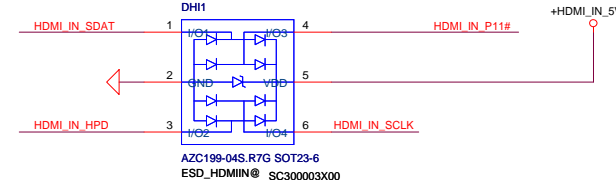
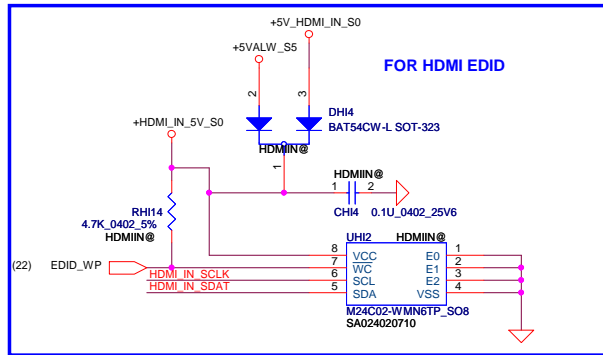
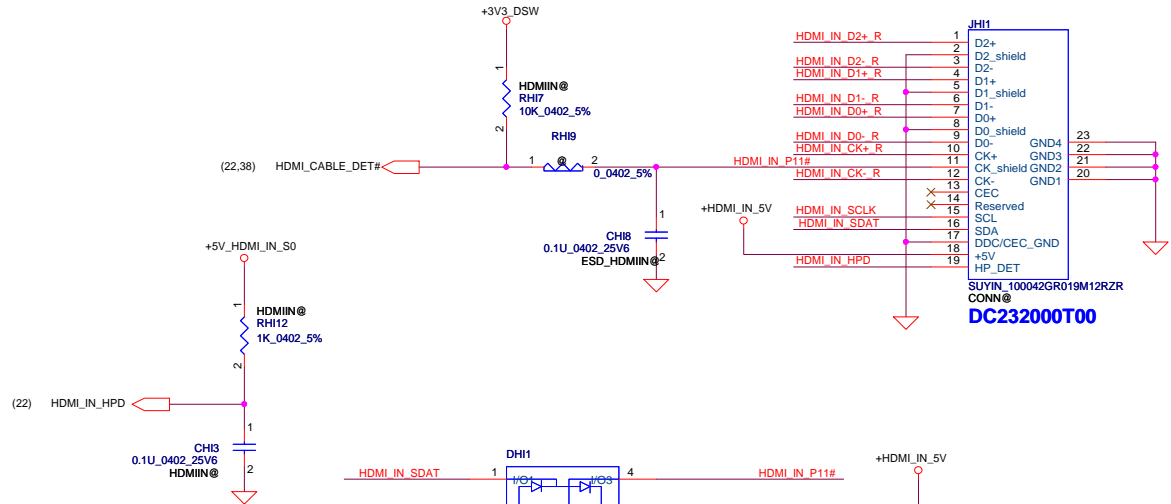
		Pin 45	
		0	1
Pin 46	0	X	
	1	EP Mode	EEPROM

		Pin 47	
		0	1
Pin 48	0	X	EP Mode
	1	EEPROM	EEPROM



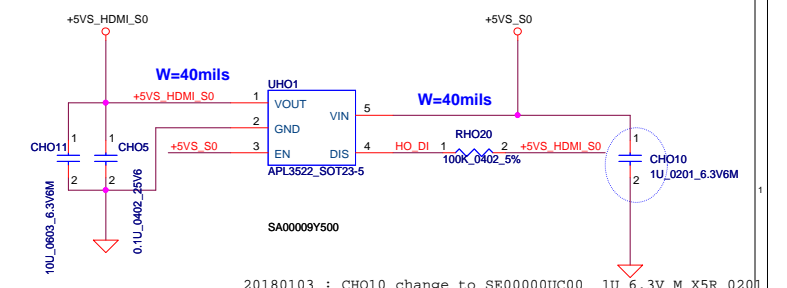
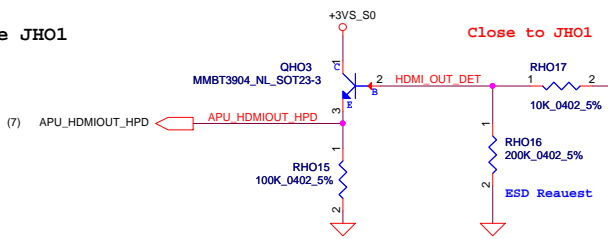
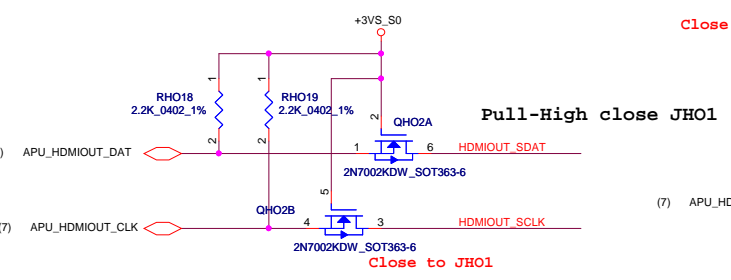
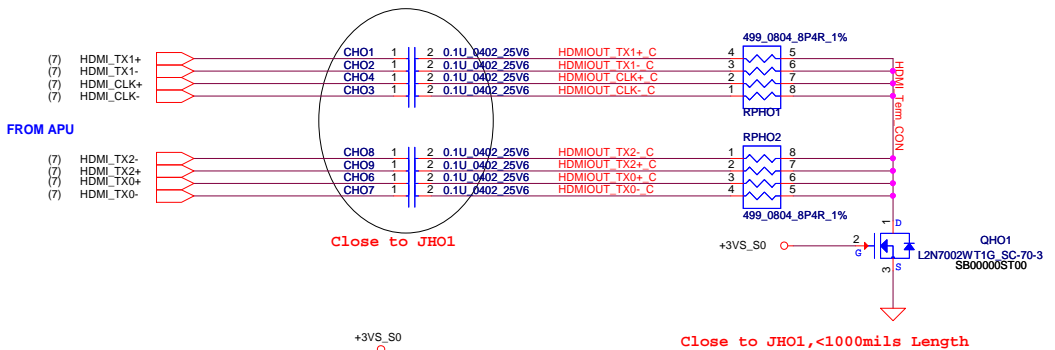
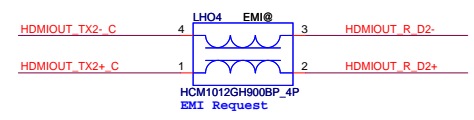
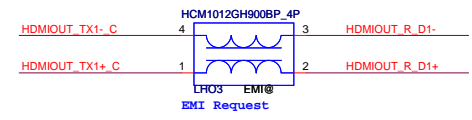
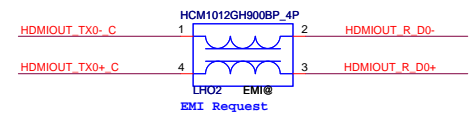
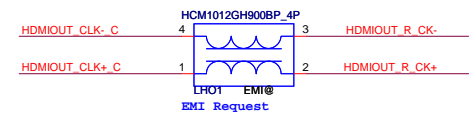


HDMI-in Connector

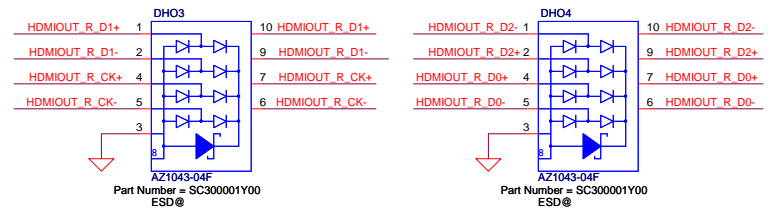
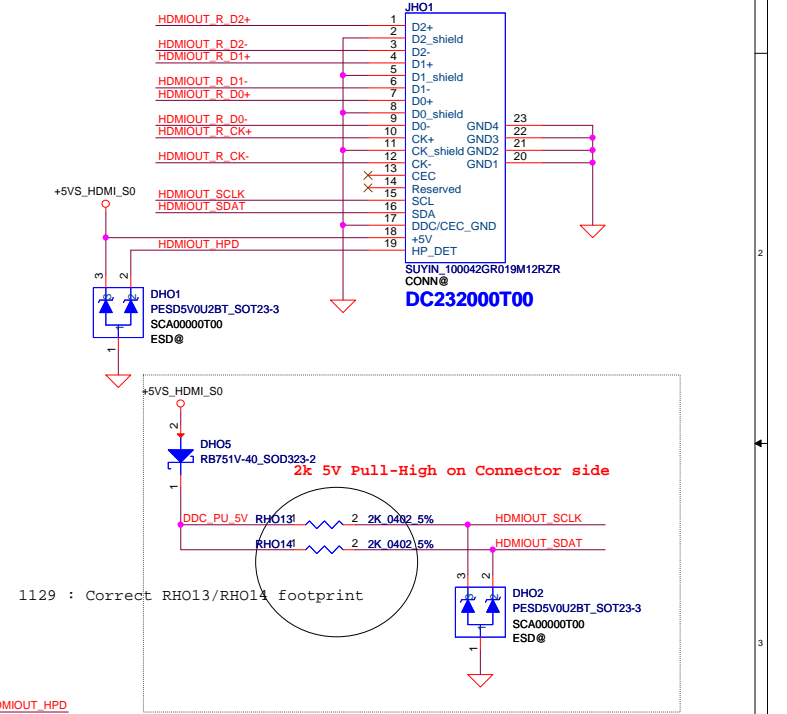


0918 Change DHI2/DHI3 main source to SC300001Y00

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Issued Date	2014/09/24	Deciphered Date	2016/09/24	Title	HDMI-IN
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Size	Custom	Document Number	LA-F902P		Date
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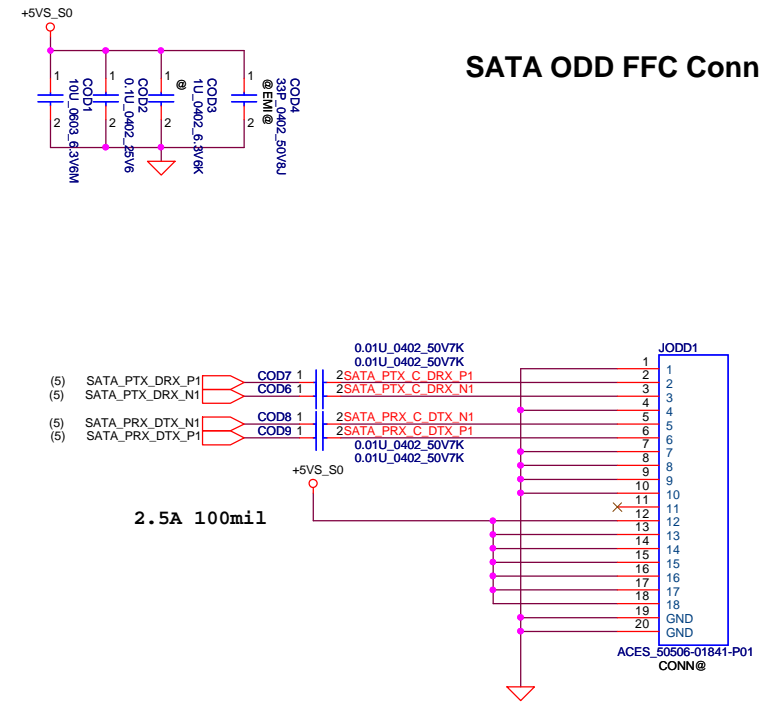
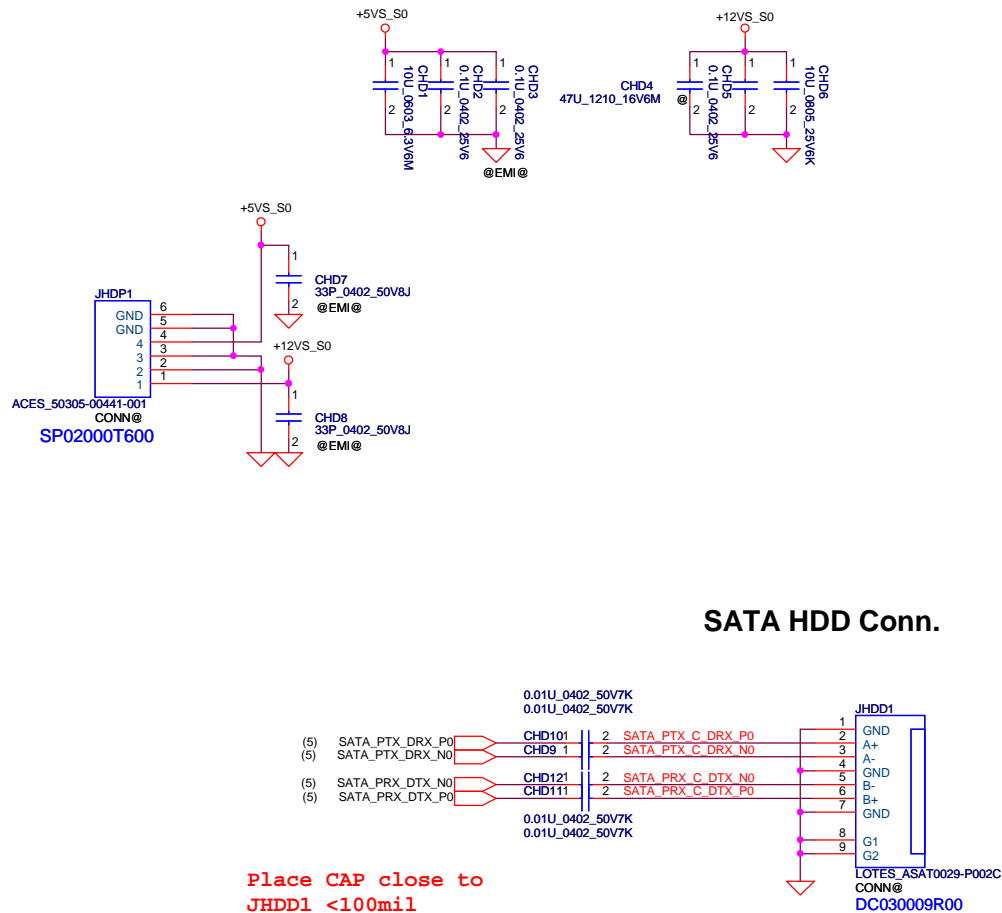


HDMI-OUT Connector



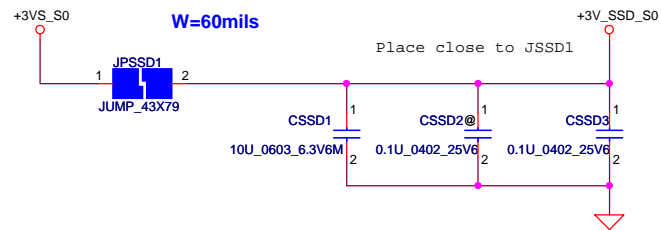
0918 Change DHO3/DHO4 main source to SC300001Y00

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Issued Date		2014/04/02		Deciphered Date		2015/10/02		Title		HDMI OUT			
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										LA-F902P		1A	
								Date		Thursday, March 22, 2018		Sheet	



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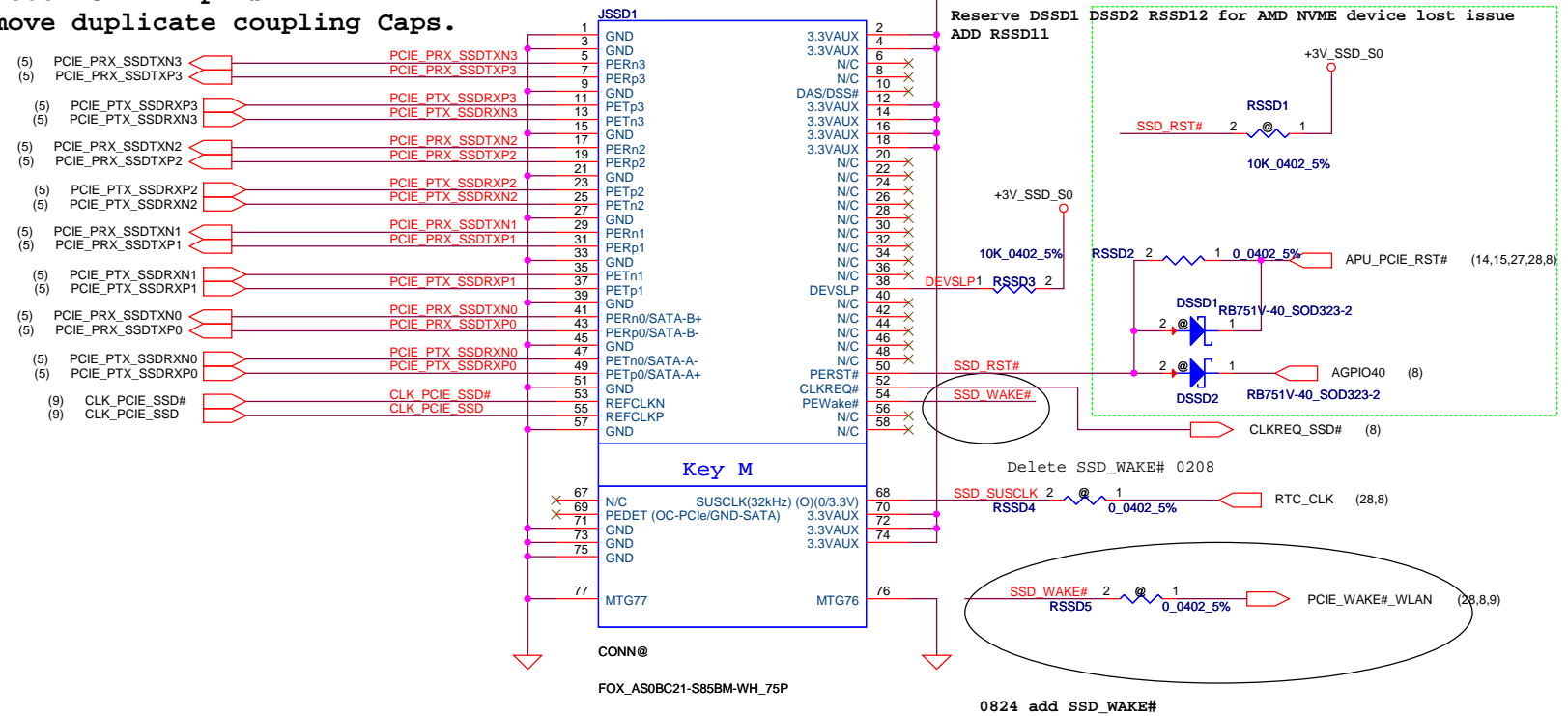
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Issued Date	2015/01/23	Deciphered Date	2017/01/23	Title	HDD/ODD
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				Date	Thursday, March 22, 2018
				Sheet	26 of 58
				Rev	1A



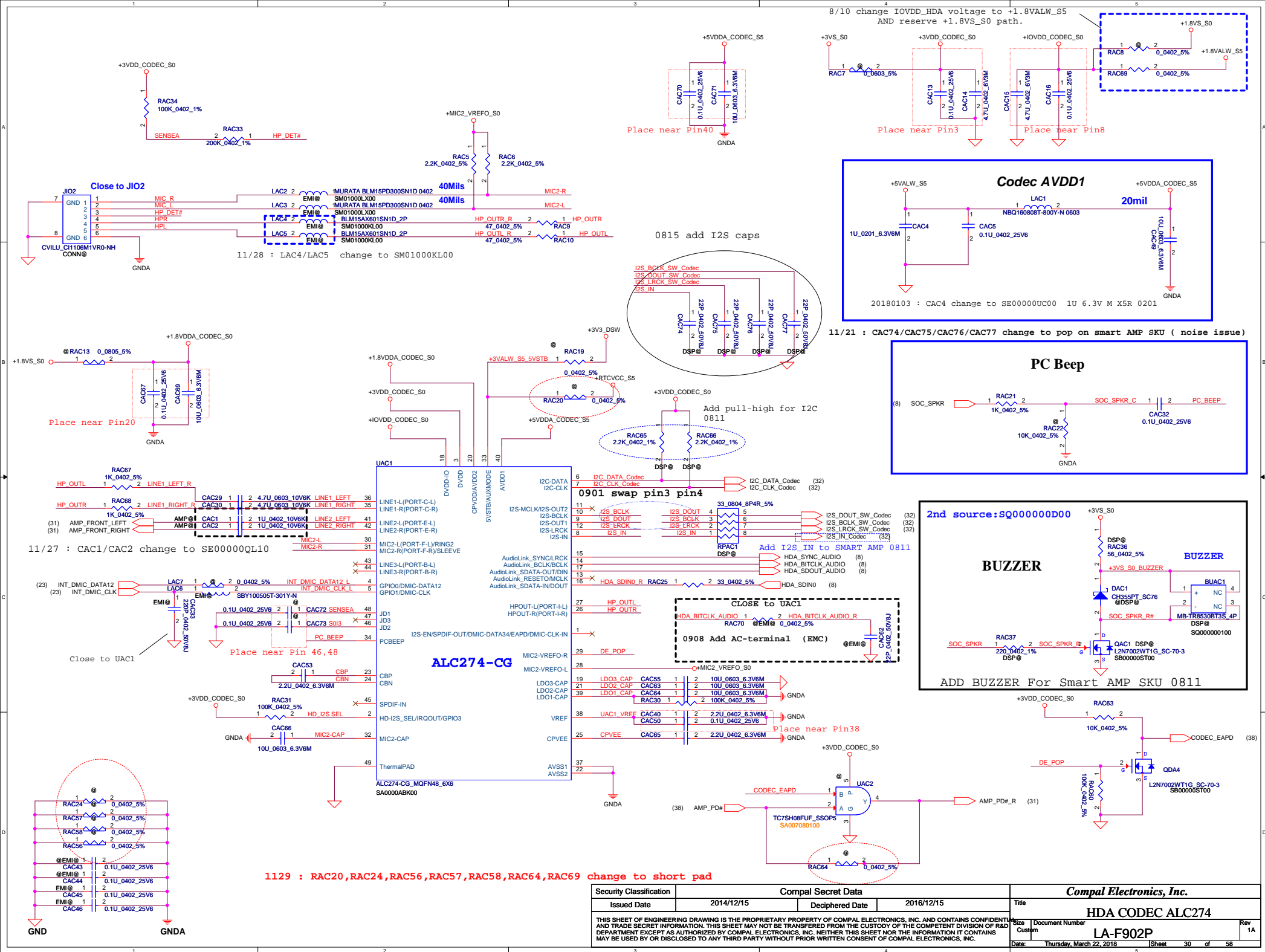
NGFF KEY M (SSD)

8/8 Correct PCIE TX pins

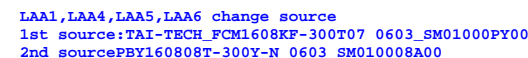
8/18 remove duplicate coupling Caps.



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/09/01	Deciphered Date	2013/09/01	Title	SSD (M2) - PCIE SSD	
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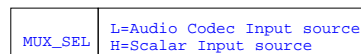


Security Classification		Compal Secret Data		Compal Electronics, Inc. HDA CODEC ALC274		
Issued Date	2014/12/15	Deciphered Date	2016/12/15	Title		
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11/27 : CAA35/CAA38 change to SE000000L10

11/28 : LAA1/LAA4/LAA5/LAA6
change to SM01000PY00FCM1608KF-300T07 0603

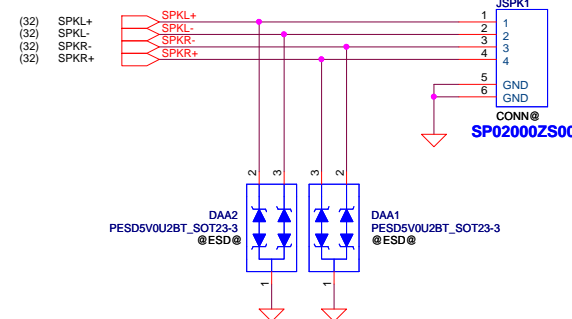


Close to UAA1 Pin17

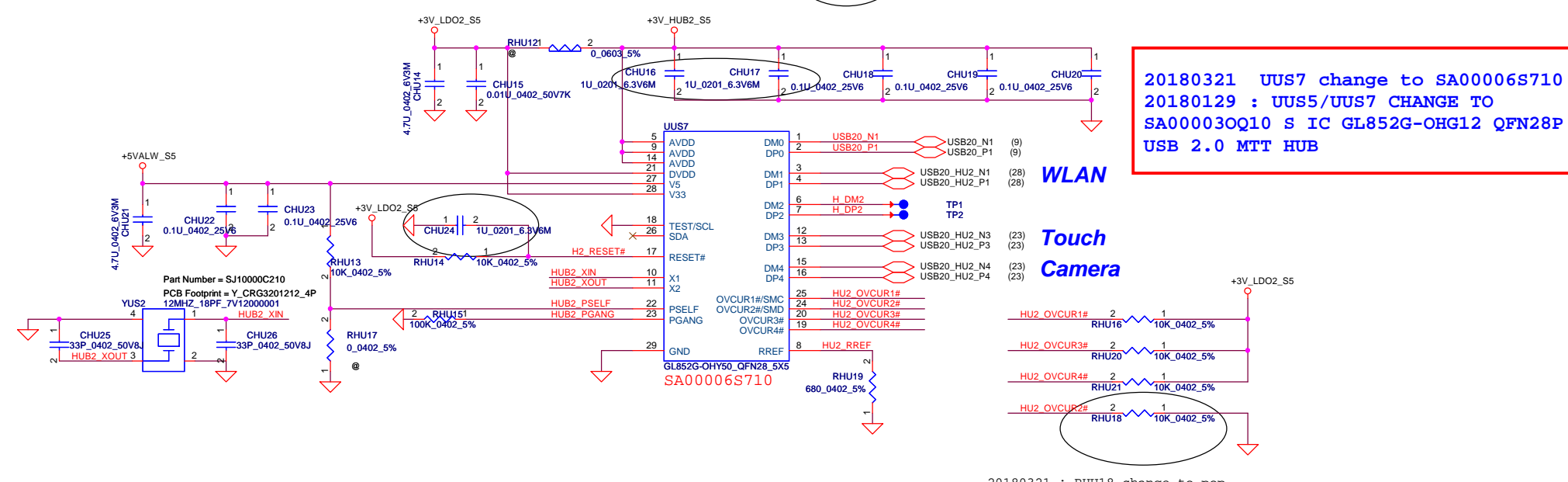
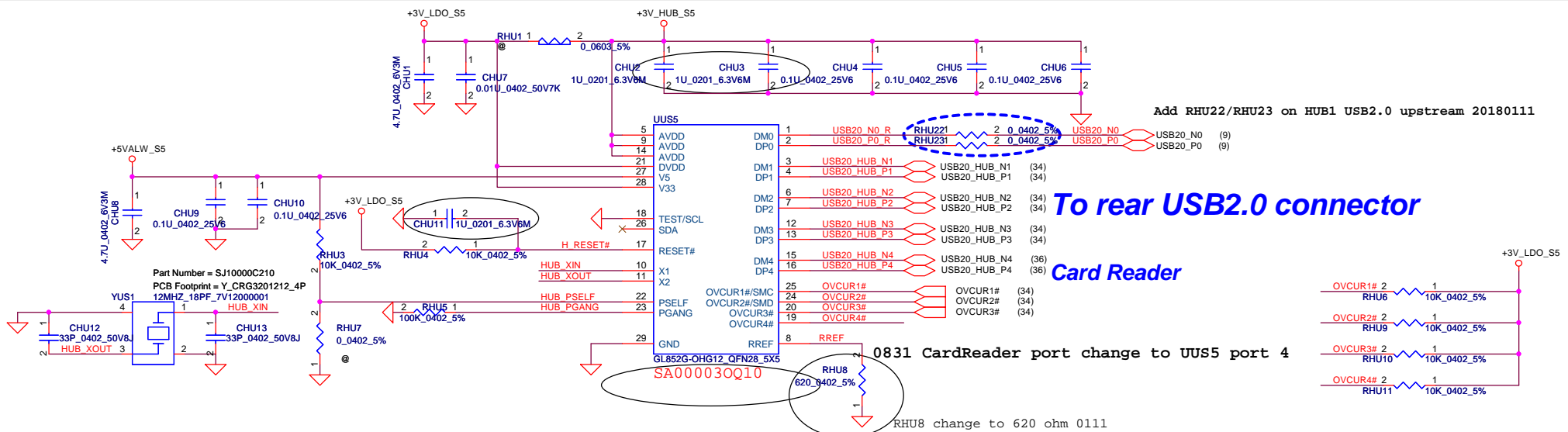
Speaker Conn
3Wx2 4ohm Speake

GAIN1	GAIN0	AV (inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

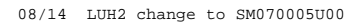
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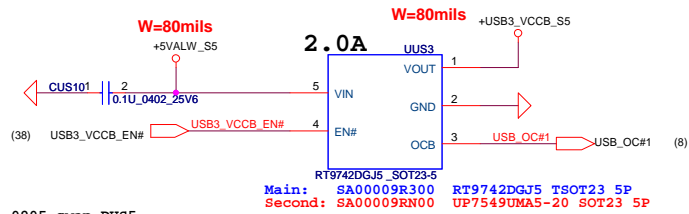
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Issued Date	2014/12/15	Deciphered Date	2016/12/15	Title		
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				Custm	AIO530	1A
				Date:	Thursday, March 22, 2018	Sheet 31 of 58



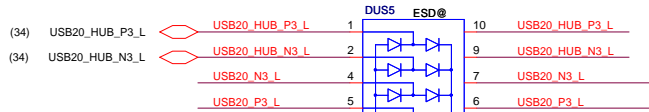
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Issued Date	2014/01/20	Deciphered Date	2015/01/20	Title	
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Size	Custom	Document Number	LA-F902P	Rev	
Date:	Thursday, March 22, 2018	Sheet	33	of 58	



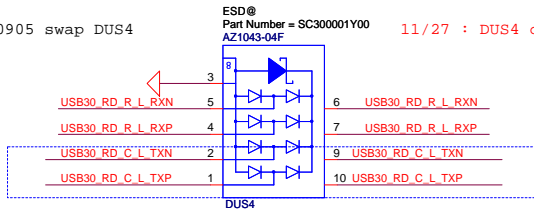
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Issued Date	2015/12/25	Deciphered Date	2016/09/24	Rear USB2.0 x 3			
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				Date: Thursday, March 22, 2018	Sheet 34	of 58	



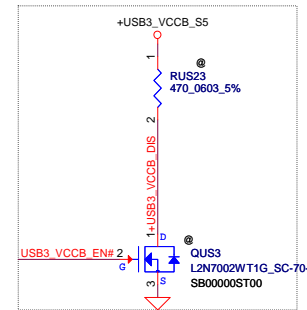
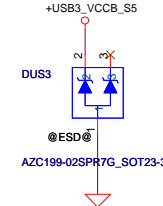
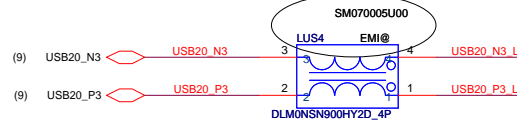
0905 swap DUS5



0905 swap DUS4

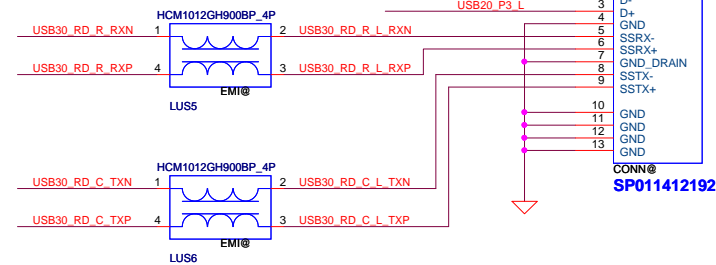


08/14 LUS4 change to SM070005U00

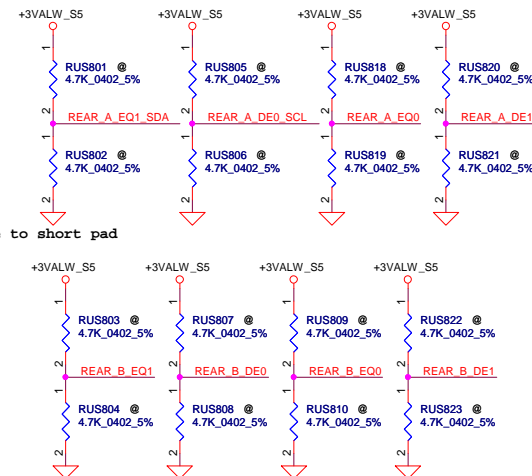
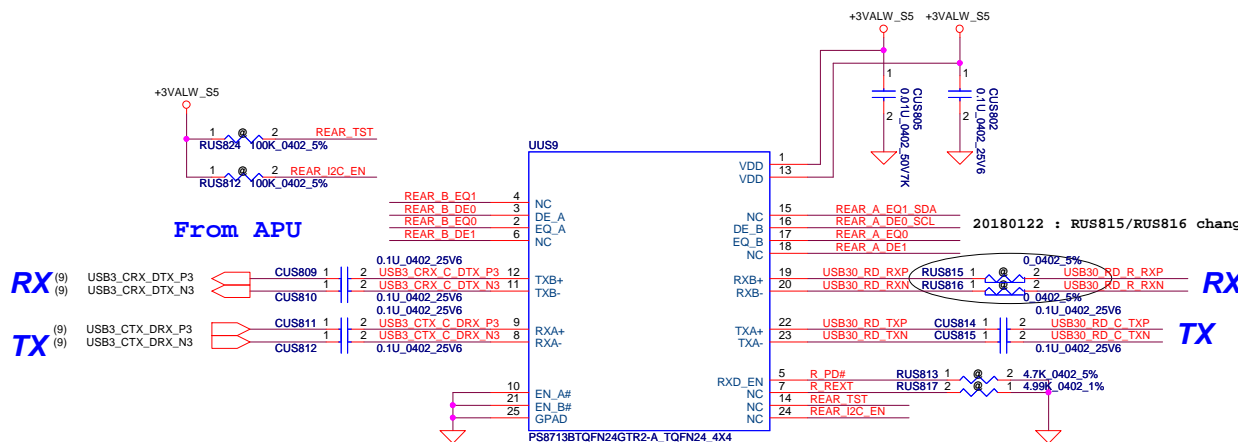


0915 USB discharge change to unpop

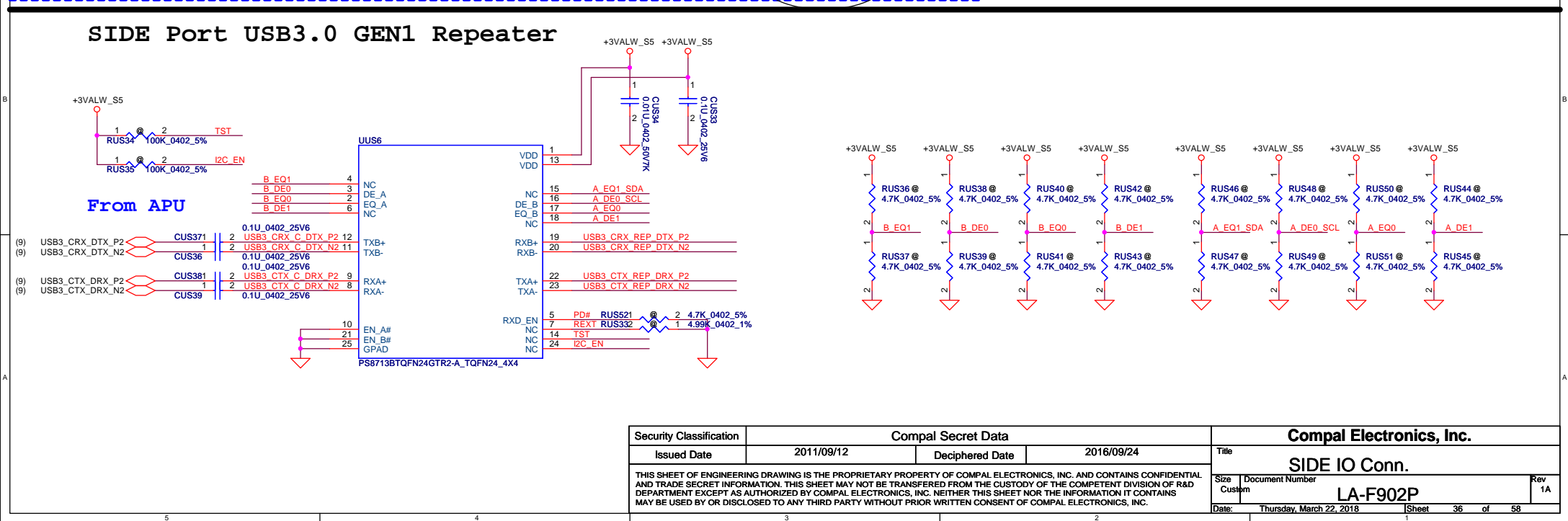
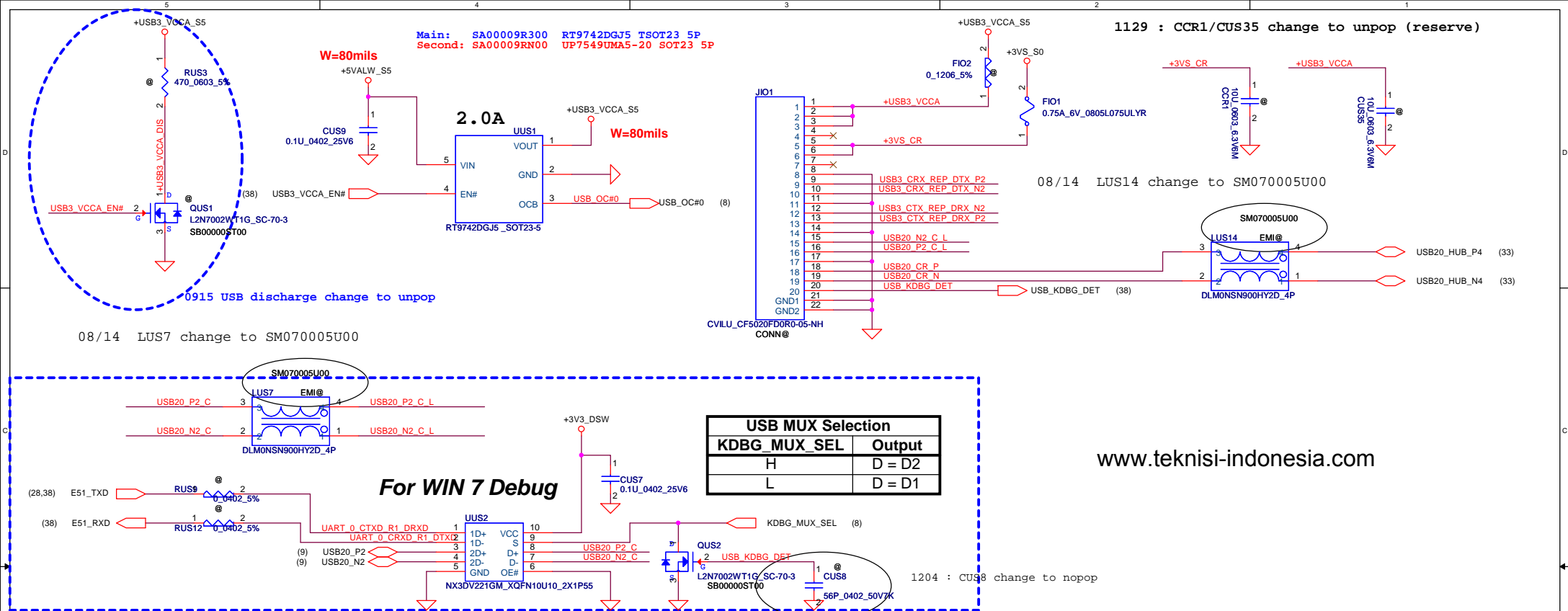
USB3.0 Conn.

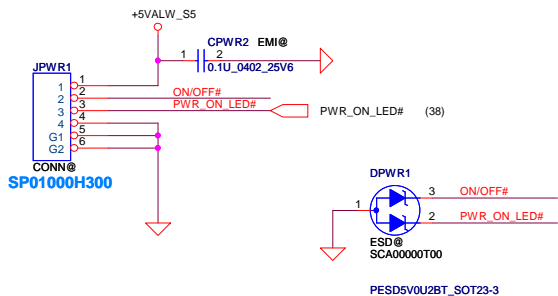


11/27 : Redriver change to PS8713

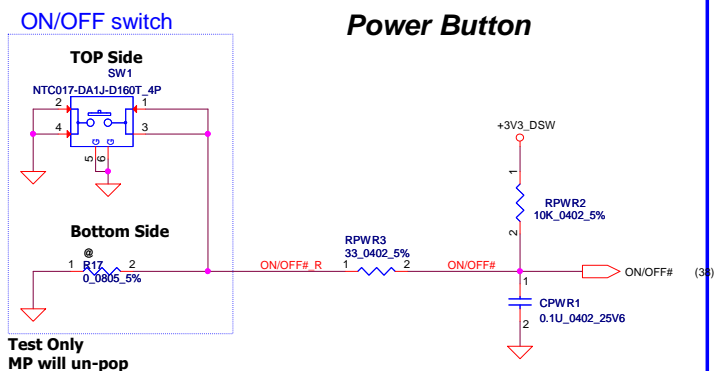
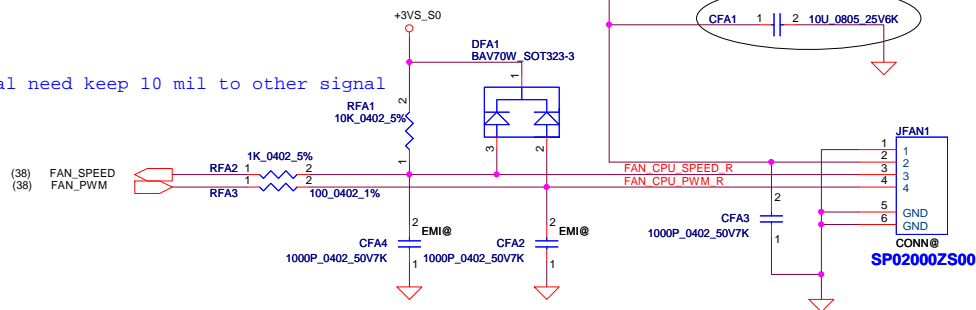


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Issued Date	2015/12/25	Deciphered Date	2016/09/24	Title
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Size	Custom	Document Number	LA-F902P	Rev 1A
Date:	Thursday, March 22, 2018	Sheet	35	of 58

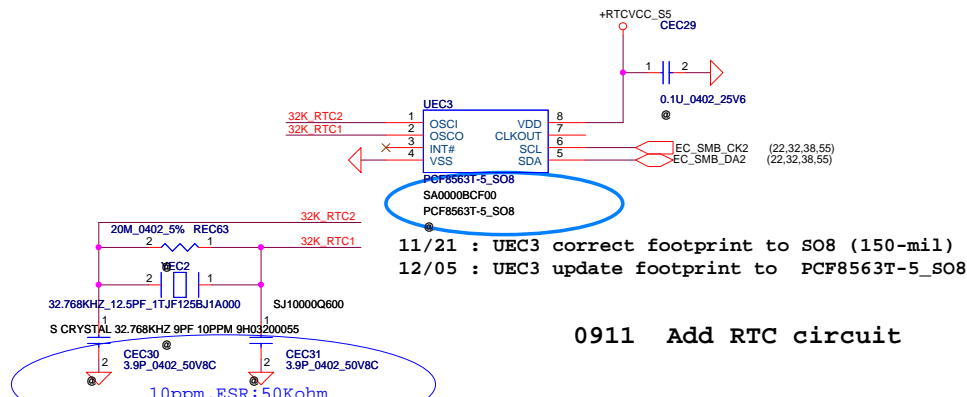




FAN_PWM signal need keep 10 mil to other signal



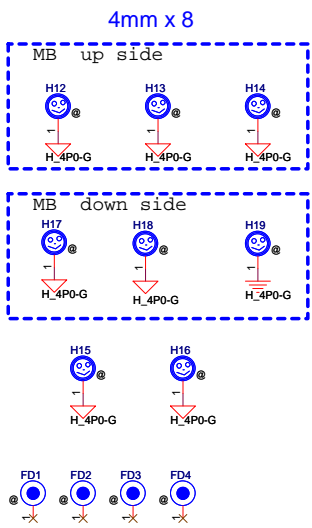
RTC EC



0911 Add RTC circuit

1206: CEC30/CEC31 change to 3.9P

Screw Hole



CPU Hole

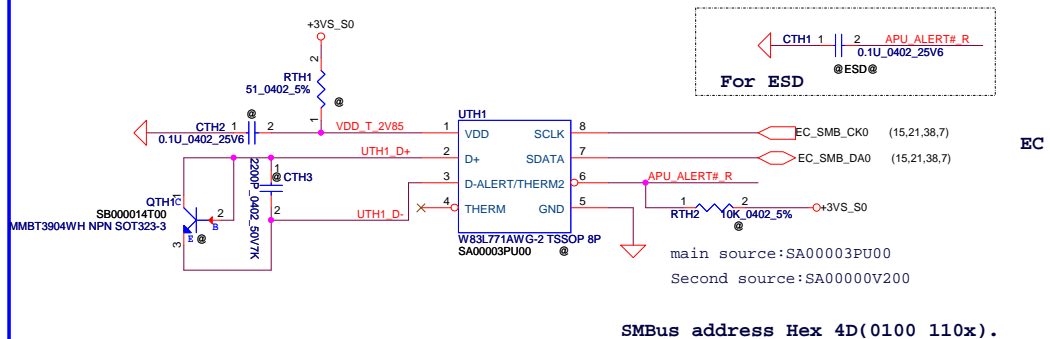
WIFI Hole

3.8mm x 4

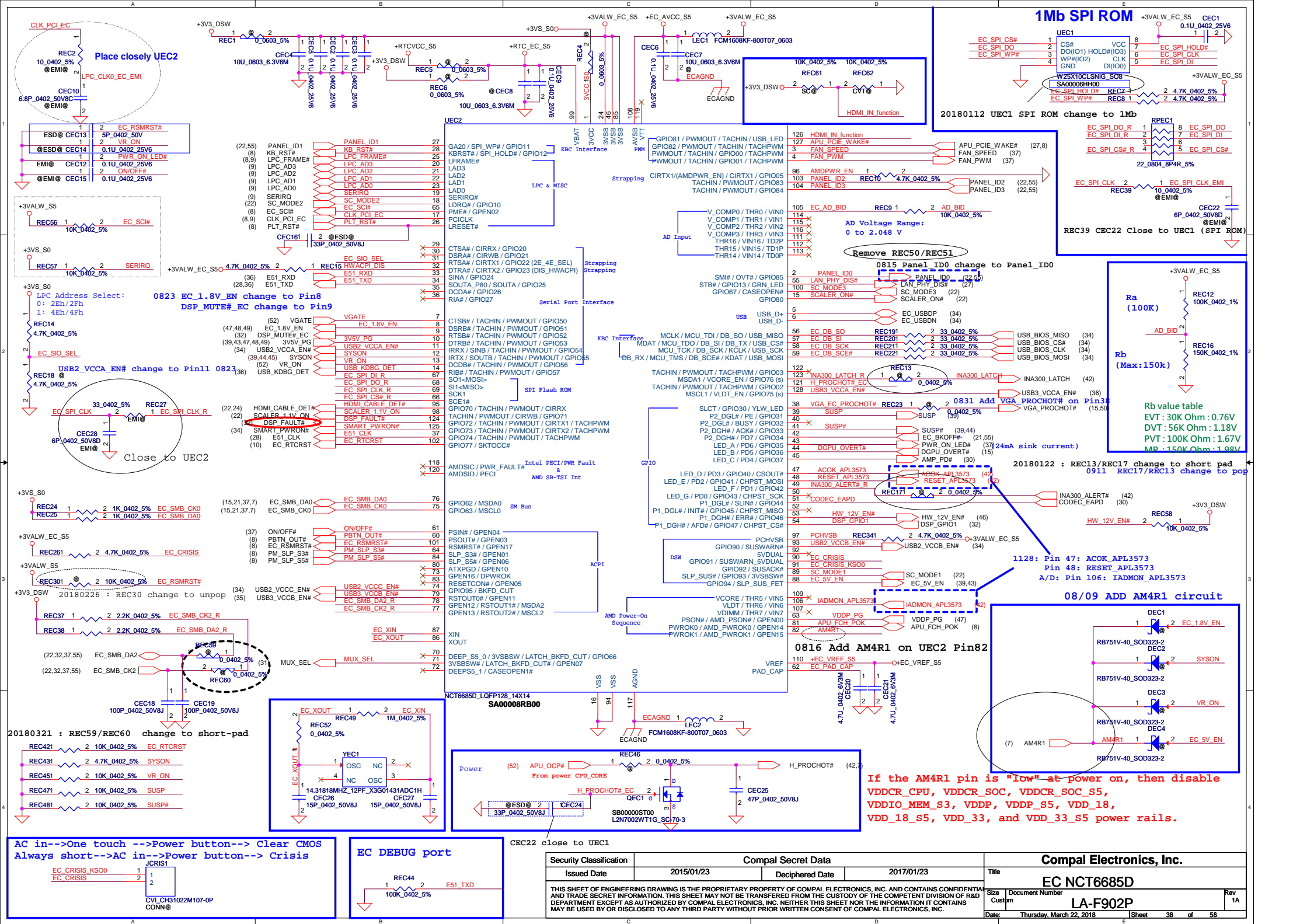
GPU Hole

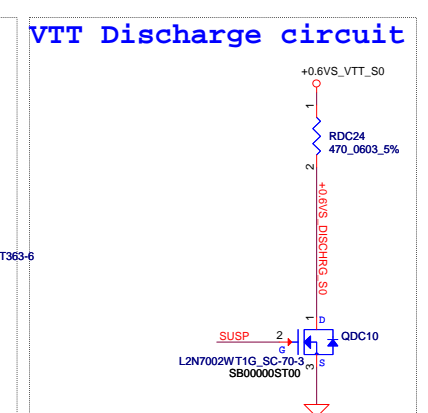
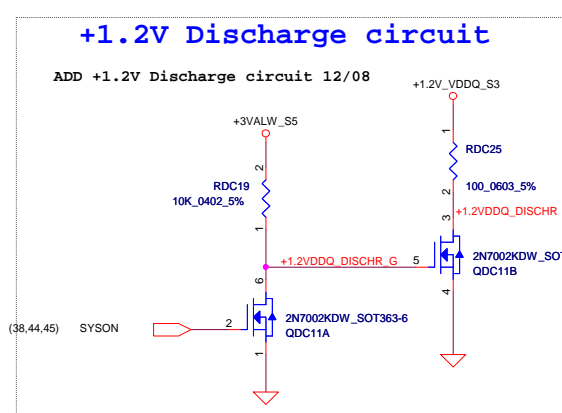
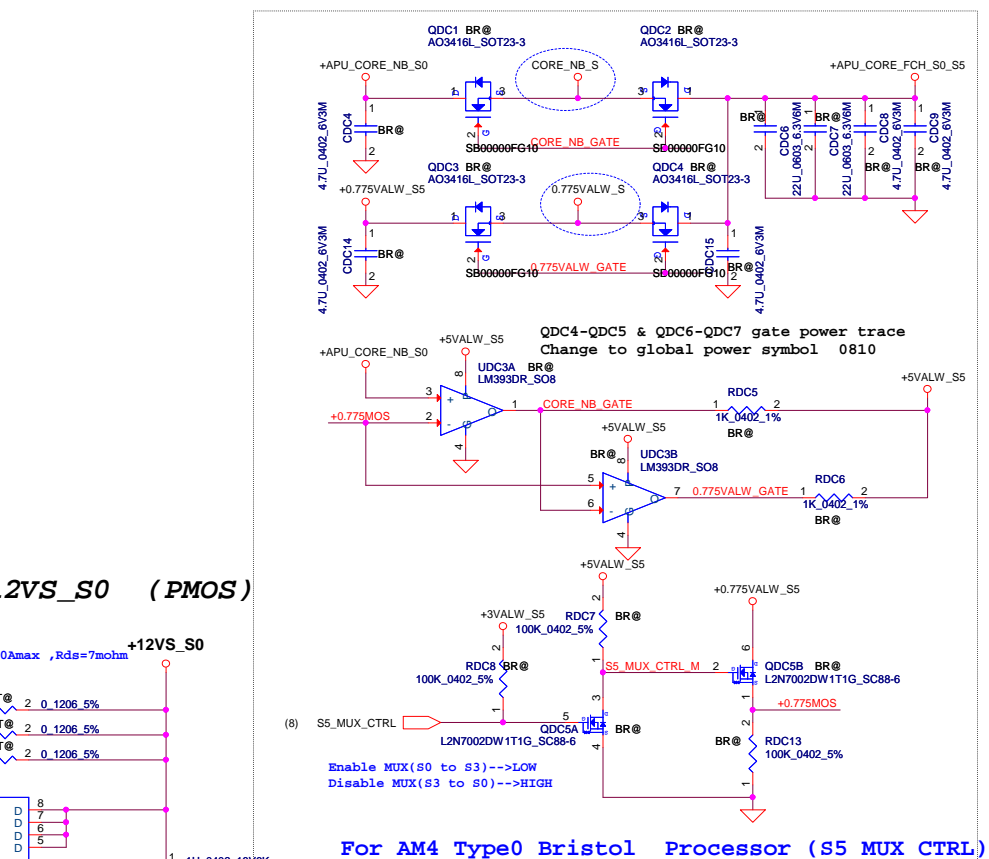
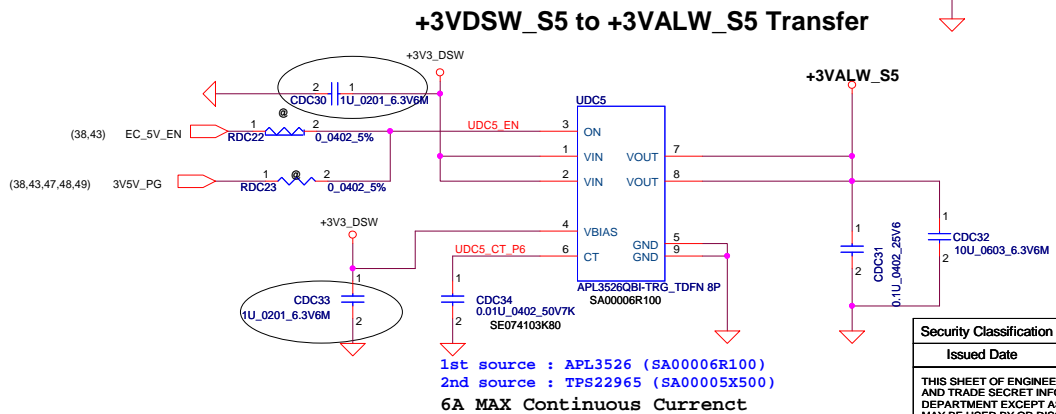
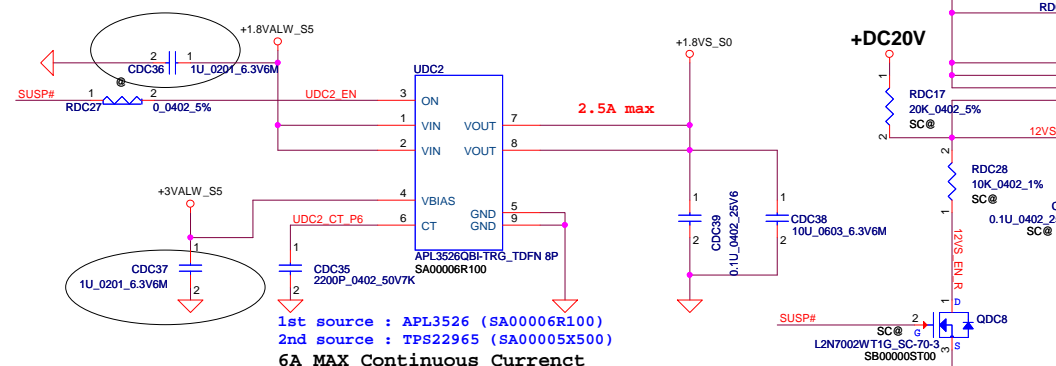
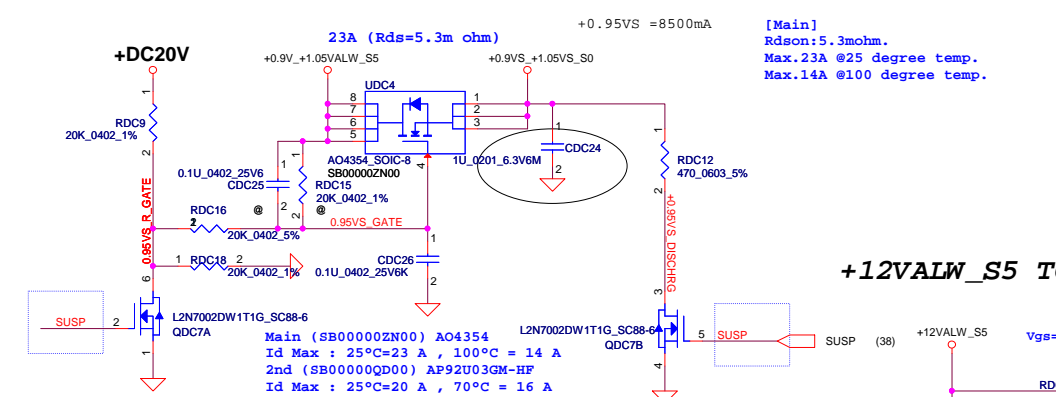
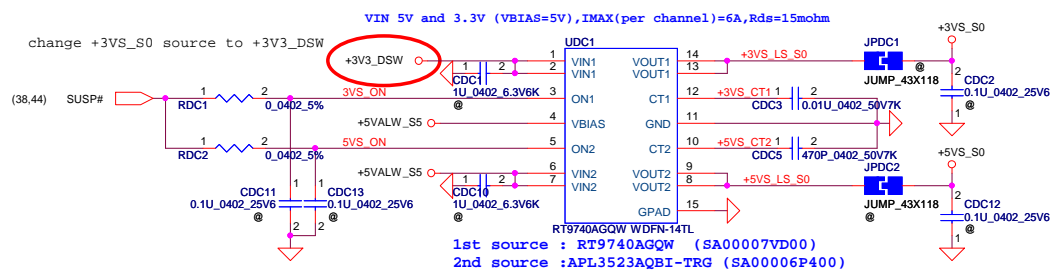
SSD Hole

3.3mm x 4



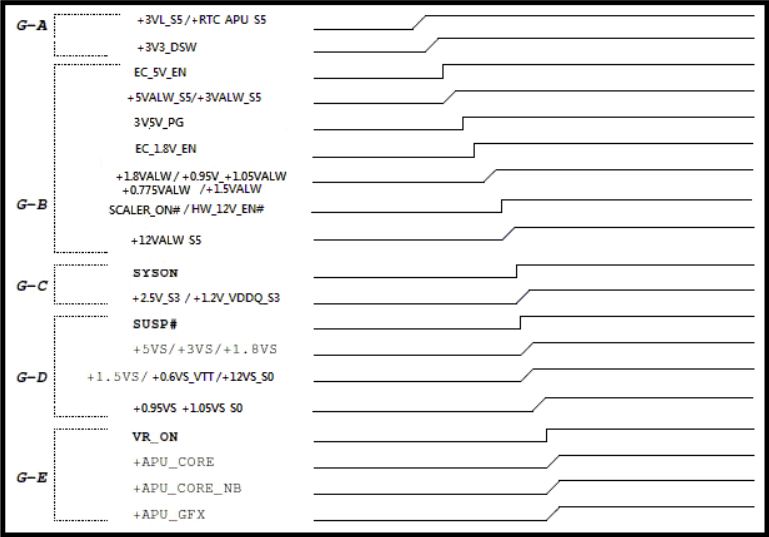
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/09/12		Deciphered Date		2012/09/12		Title		PWR Conn./FAN/Thermal/SCREW	
Size		Document Number		Date		Thursday, March 22, 2018		Sheet		37 of 58	
Custom		LA-F902P		Rev		1A					



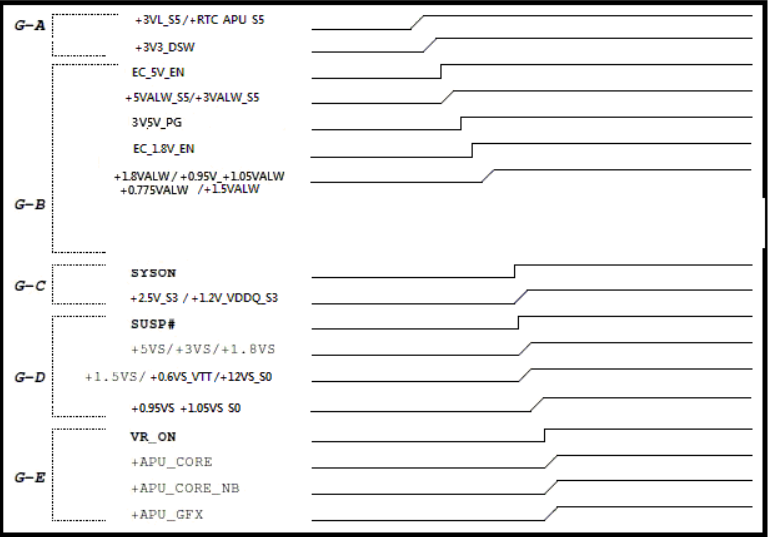


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Issued Date	2015/01/23	Deciphered Date	2017/01/23	DC INTERFACE	
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				Custom	LA-F902P
				Date:	Thursday, March 22, 2018
				Sheet	39 of 58
				Rev	1A

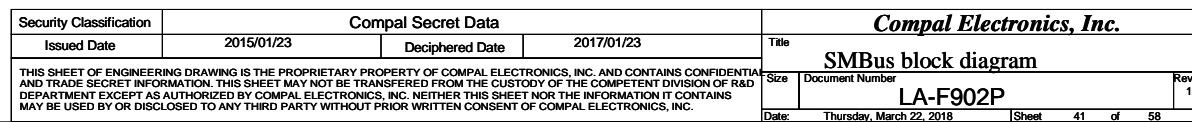
POWER SEQUENCE (For Scaler SKU)



POWER SEQUENCE (For CVT SKU)



APU



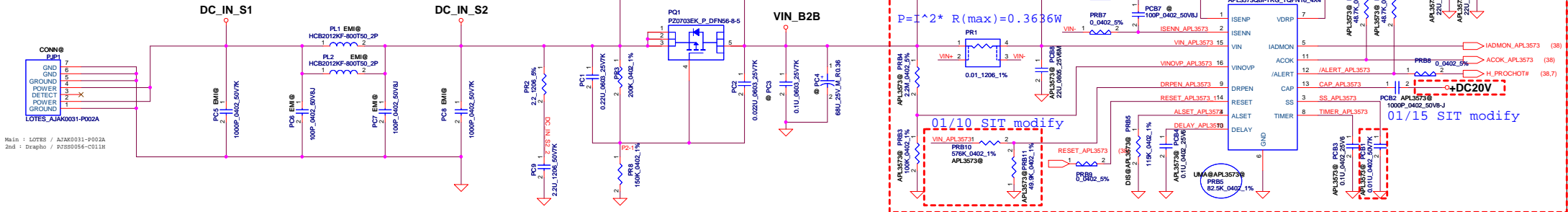
Main source: PZ0703EK
 $PD = I^2 \cdot R_{ds(on)} = 6^2 \cdot 7m \text{ ohm} = 0.252W$
 $\theta JA = 50^\circ C/W \cdot 0.252W = 12.6^\circ C$
 Second source: AON6405L
 $PD = I^2 \cdot R_{ds(on)} = 6^2 \cdot 7m \text{ ohm} = 0.252W$
 $\theta JA = 50^\circ C/W \cdot 0.252W = 12.6^\circ C$
 Third source: SIR403EDP-T1-GE3
 $PD = I^2 \cdot R_{ds(on)} = 6^2 \cdot 6.5m \text{ ohm} = 0.234W$
 $\theta JA = 50^\circ C/W \cdot 0.468W = 11.7^\circ C$

01/10 SIT add
 W/O APL3573 open
 W/ APL3573 short

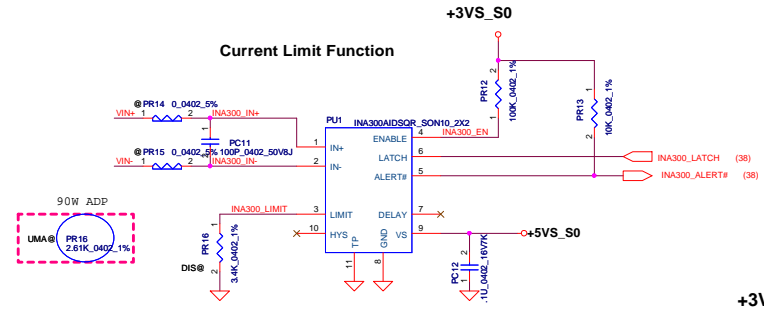
11/28 SDV add APL3573 circuit

W/O INA300 : PL3, PL4 pop
 W/ INA300: PRI pop

W/O APL3573 short
 W/ APL3573 open

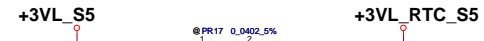
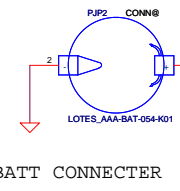


Current Limit Function



90W:
 Full Load(100%) --> 4.5A
 $V_{trip} = 4.5 \cdot 10m = 45mV$
 $V_{Limit} = V_{trip}$; $R_{limit} = (45mV + 0.5mV) / 20uA = 2.275K$
 Trigger(116.7%) --> 5.25A (@105W)
 $V_{trip} = 5.25 \cdot 10m = 52.5mV$
 $R_{limit} = (52.5mV + 0.5mV) / 20uA = 2.65K$
 Select $R_{limit} = 2.61K$
 $I_{Trigger} \rightarrow 5.22A$

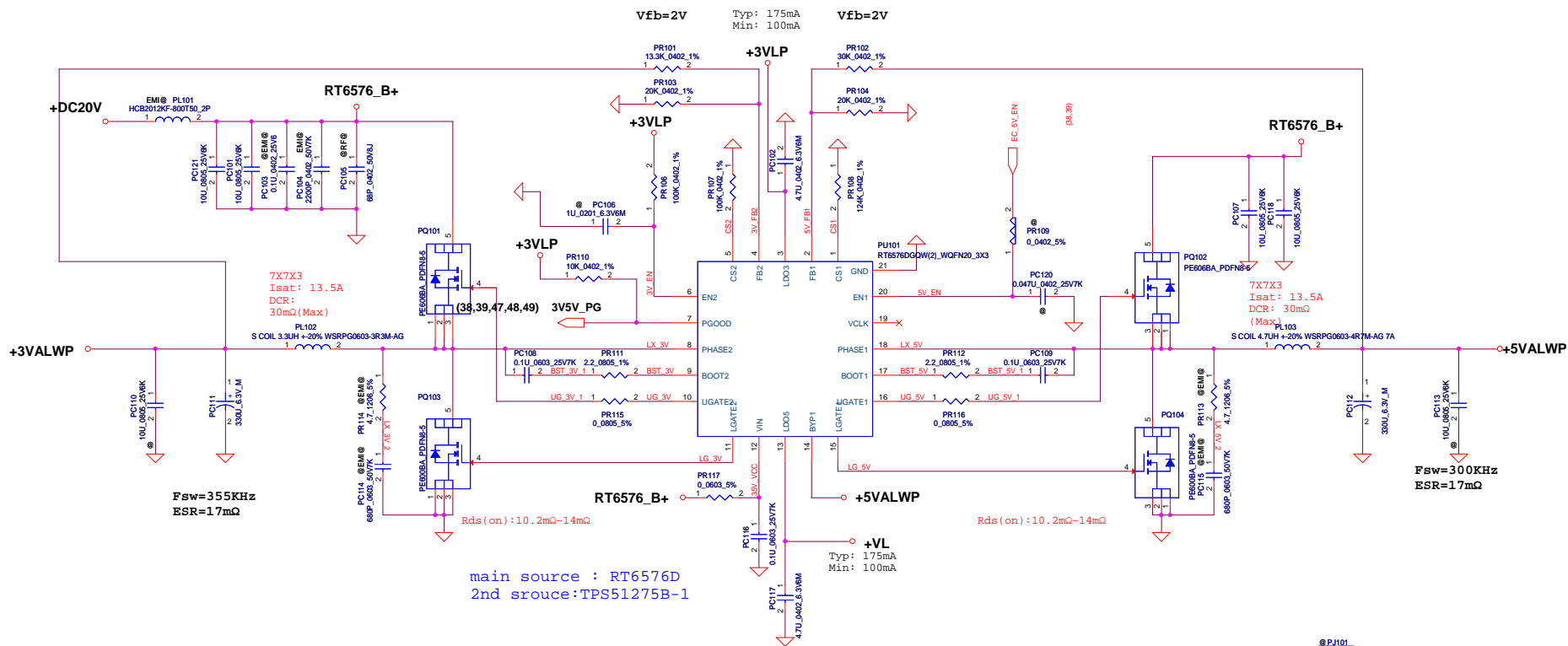
120W:
 Full Load(100%) --> 6A
 $V_{trip} = 6 \cdot 10m = 60mV$
 $V_{Limit} = V_{trip}$; $R_{limit} = (60mV + 0.5mV) / 20uA = 3.025K$
 Trigger(115%) --> 6.9A (@138W)
 $V_{trip} = 6.9 \cdot 10m = 69mV$
 $R_{limit} = (69mV + 0.5mV) / 20uA = 3.475K$
 Select $R_{limit} = 3.4K$
 $I_{Trigger} \rightarrow 6.75A$



DIS SKU 120W:
 Peak Load --> 7.5A (@150W)
 $Valset = 7.5A \cdot 10mohm \cdot 15.4 = 1.155V$
 $Ralset = 1.155V / 10uA = 115.5K$
 Select $Ralset = 115K$
 $Tdebounce_alert = 0.1uF / 10uA = 10ms$

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				Customer		0-1	



$$+3VALWP$$

$$V_{in} = 20V$$

$$I_{in} = 3.3 \times 6.4 / 20 / 0.85 = 1.24A$$

$$V_{out} = V_{fb} \times [1 + (R_t/R_b)]$$

$$= 2 \times [1 + (13.3K/20K)] = 3.3V$$

$$+3VALWP$$

$$I_{peak} = 6.4A ; I_{tdc} = 4.48A ; F_{sw} = 355KHz$$

$$I_{ocp} = (R_{cs1} \times I_{trip}) / (8 \times R_{dson})$$

$$R_{ds} : L/S \rightarrow typ: 10.2m\Omega ; max: 14m\Omega$$

$$I_{trip} = 9-11 \mu A$$

$$I_{ocp}(set) = I_{ocp}(set) = 10.3A-12.7A$$

$$I_{in_ripple} = 1.66A$$

$$Output\ Cap. ESR = 17m\Omega$$

$$\Delta IL = [(V_{in} - V_o) / L] \times [(V_{out} / V_{in}) \times T] = 2.352A$$

$$LIR = \Delta IL / I_{peak} = 0.36$$

$$C_{out} = [L \times (I_{out} + \Delta IL / 2)^2] / [(V_{out} + \Delta V)^2 - V_{out}^2] = 240\mu F$$

$$CINBULK = I_{Load} \times V_{out} \times (V_{in} - V_{out}) / (F_{sw} \times V_{in}^2 \times VINPP) = 0.87\mu F$$

$$+5VALWP$$

$$V_{in} = 20V$$

$$I_{in} = 5 \times 8 / 0.85 / 20 = 2.35A$$

$$V_{out} = V_{fb} \times [1 + (R_t/R_b)]$$

$$= 2 \times [1 + (30K/20K)] = 5V$$

$$+5VALWP$$

$$I_{peak} = 8A ; I_{tdc} = 5.6A ; F_{sw} = 300KHz$$

$$I_{ocp} = (R_{cs1} \times I_{trip}) / (8 \times R_{dson})$$

$$R_{ds} : L/S \rightarrow typ: 10.2m\Omega ; max: 14m\Omega$$

$$I_{trip} = 9-11 \mu A$$

$$I_{ocp}(set) = 12A-14A$$

$$I_{in_ripple} = 2.42A$$

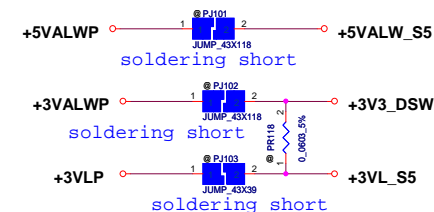
$$Output\ Cap. ESR = 17m\Omega$$

$$\Delta IL = [(V_{in} - V_o) / L] \times [(V_{out} / V_{in}) \times T] = 2.66A$$

$$LIR = \Delta IL / I_{peak} = 0.33$$

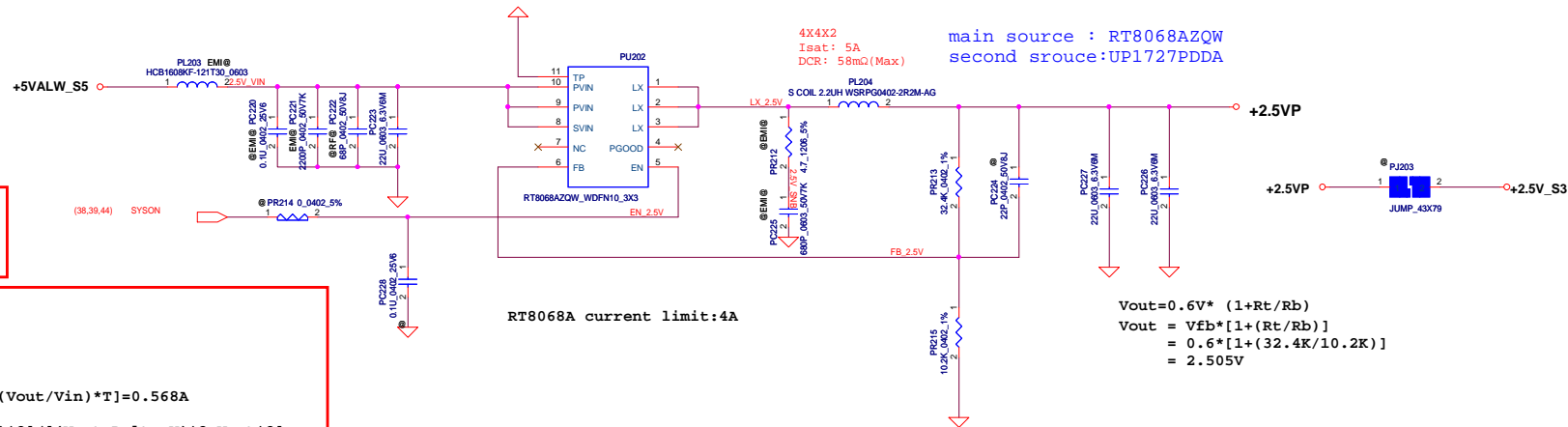
$$C_{out} = [L \times (I_{out} + \Delta IL / 2)^2] / [(V_{out} + \Delta V)^2 - V_{out}^2] = 223\mu F$$

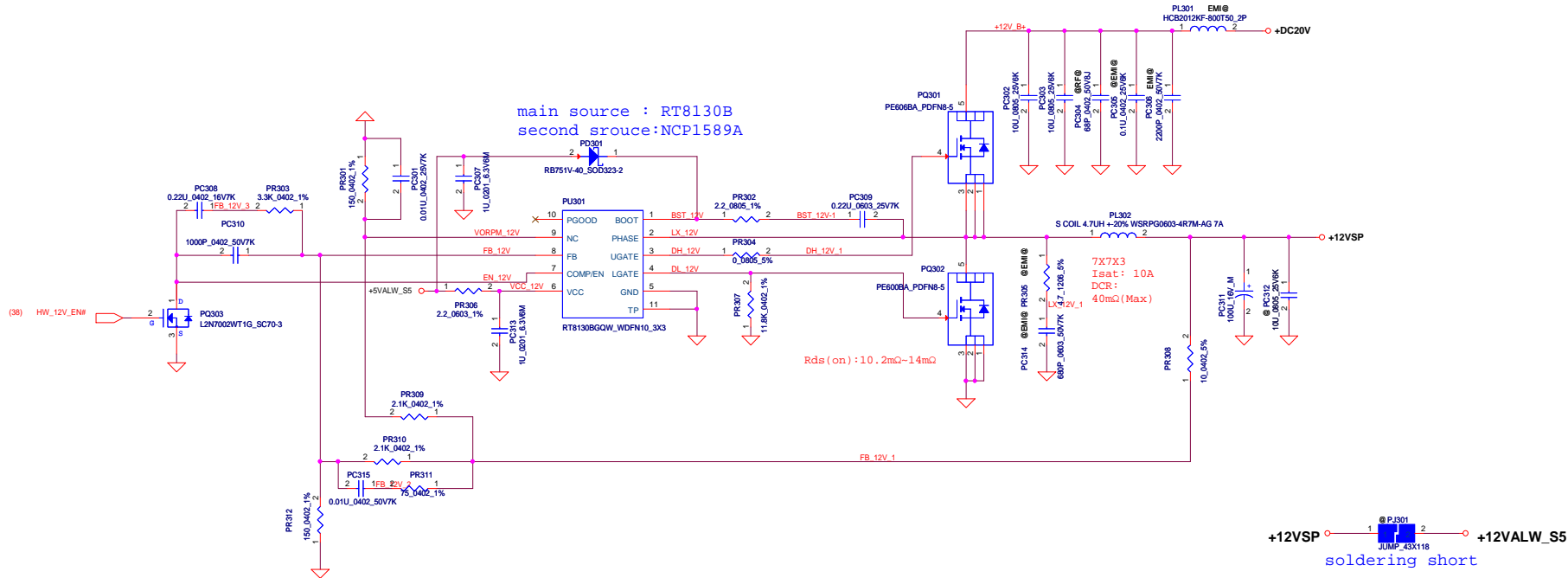
$$CINBULK = I_{Load} \times V_{out} \times (V_{in} - V_{out}) / (F_{sw} \times V_{in}^2 \times VINPP) = 1.75\mu F$$



+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A

+2.5VP
Ipeak=2.24A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF



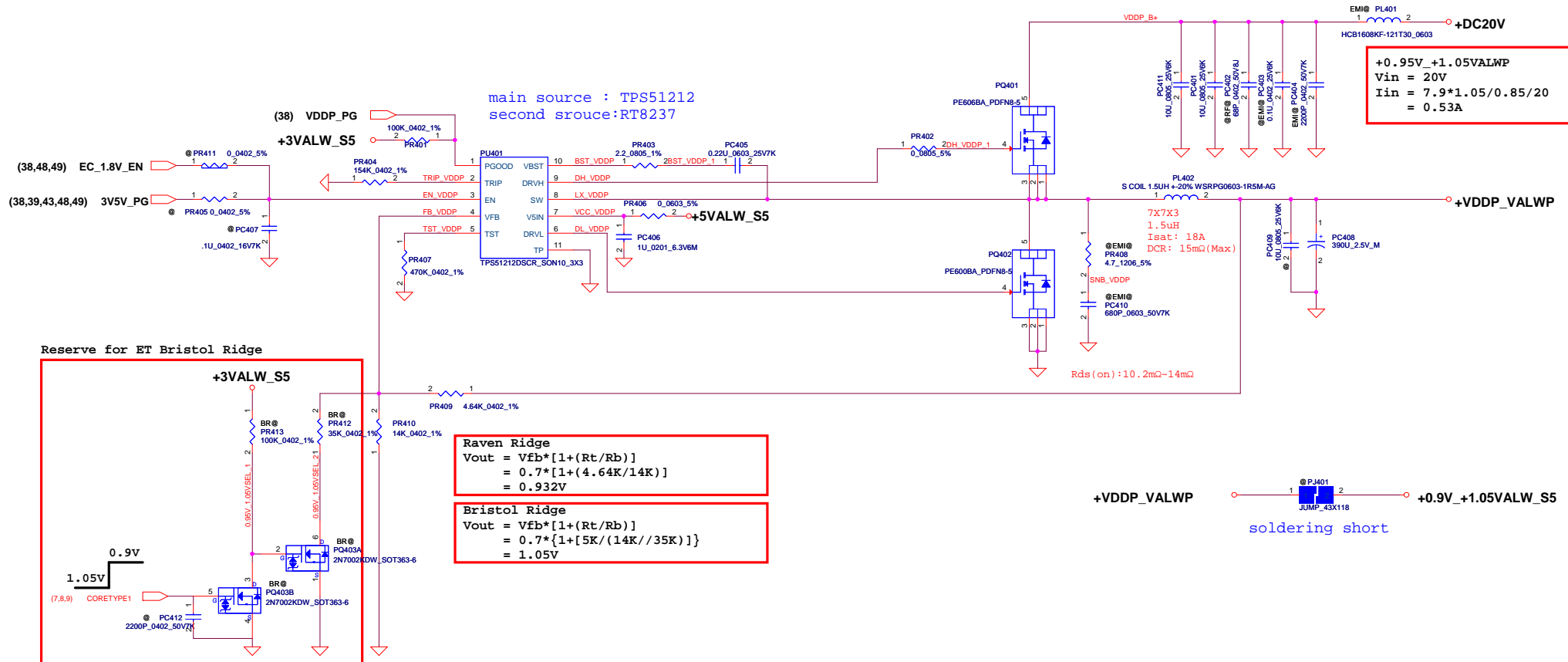


+12VSP
 $I_{max}=2.45A, I_{peak}=3.5A ; f_{sw}=300KHz$
 $I_{ocp}=(R_{cs1} \cdot I_{trip})/R_{ds(on)}$
 $R_{ds} : L/S \rightarrow typ:10.2m\Omega ; max: 14m\Omega$
 $I_{trip}=9-11 \mu A$
 $I_{ocp(set)}=10.11-11.98A$
 $I_{in_ripple}=0.615A$
 $Output\ Cap. ESR=24m\Omega$
 $\Delta IL=[(V_{in}-V_o)/L] \cdot [(V_{out}/V_{in}) \cdot T]=3.404A$
 $LIR=\Delta IL/I_{peak}=0.973$
 $C_{out}=[L \cdot (I_{out}+\Delta IL/2)^2]/[(V_{out}+\Delta V)^2-V_{out}^2]$
 $=5.49\mu F$
 $CINBULK=I_{load} \cdot V_{out} \cdot (V_{in}-V_{out})/(f_{sw} \cdot V_{in}^2 \cdot VINPP)=0.98\mu F$

$V_{out} = V_{fb} \cdot [1 + (R_t/R_b)]$
 $= 0.8 \cdot [1 + (2.1K/150)]$
 $= 12V$

+12VSP
 $V_{in} = 20V$
 $I_{in} = 12 \cdot 3.5/0.85/20$
 $= 2.47A$

main source : TPS51212
second source:RT8237



$$+0.95V_+1.05VALWP$$

$$V_{in} = 20V$$

$$I_{in} = 7.9 * 1.05 / 0.85 / 20$$

$$= 0.53A$$

Raven Ridge

$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.7 * [1 + (4.64K / 14K)]$$

$$= 0.932V$$

Bristol Ridge

$$V_{out} = V_{fb} * [1 + (R_t / R_b)]$$

$$= 0.7 * [1 + [5K / (14K // 35K)]]$$

$$= 1.05V$$

+0.95VALW

$$I_{peak} = 9.5A ; f_{sw} = 300KHz$$

$$I_{ocp} = (R_{cs1} * I_{trip}) / R_{dson}$$

$$R_{ds} : L / S \rightarrow typ: 10.2mohm ; max: 14mohm$$

$$I_{trip} = 9.11uA$$

$$I_{ocp(set)} = 14.717A \sim 17.756A$$

$$I_{in_ripple} = 1.58A$$

$$Output\ Cap.\ ESR = 10mohm$$

$$\Delta IL = [(V_{in} - V_o) / L] * [(V_{out} / V_{in}) * T] = 2.08A$$

$$LIR = \Delta IL / I_{peak} = 0.219$$

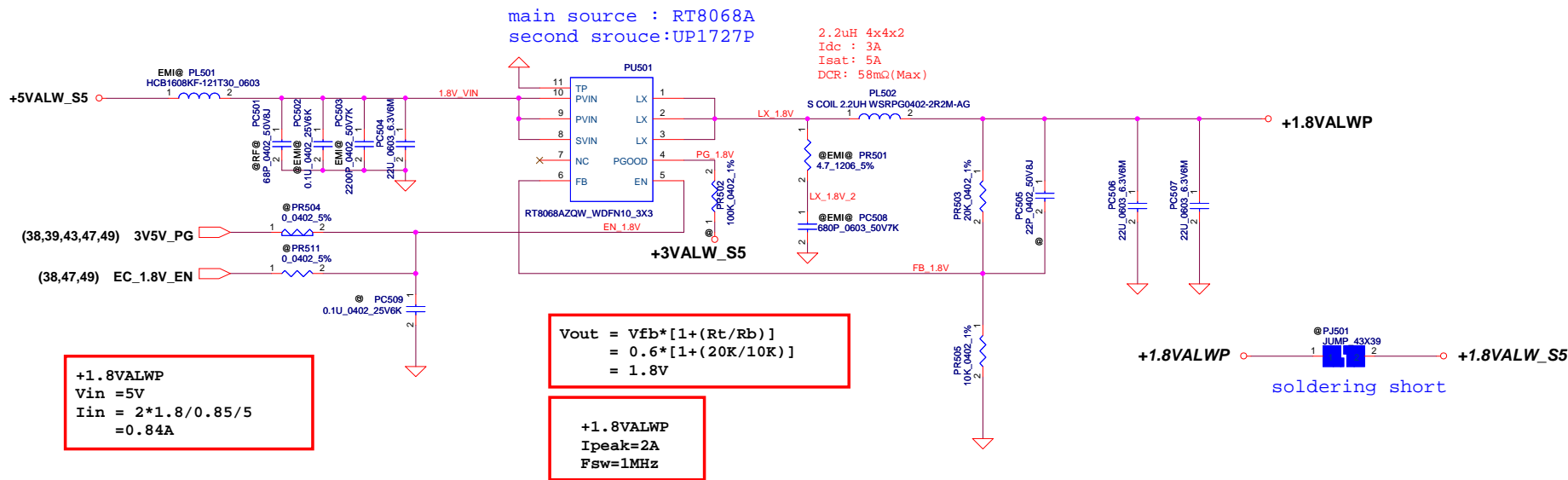
$$C_{out} = [L * (I_{out} + \Delta IL / 2) ^ 2] / [(V_{out} + \Delta V) ^ 2 - V_{out} ^ 2]$$

$$= 958uF$$

$$CINBULK = I_{load} * V_{out} * (V_{in} - V_{out}) / (f_{sw} * V_{in} ^ 2 * VINPP) = 0.52uF$$

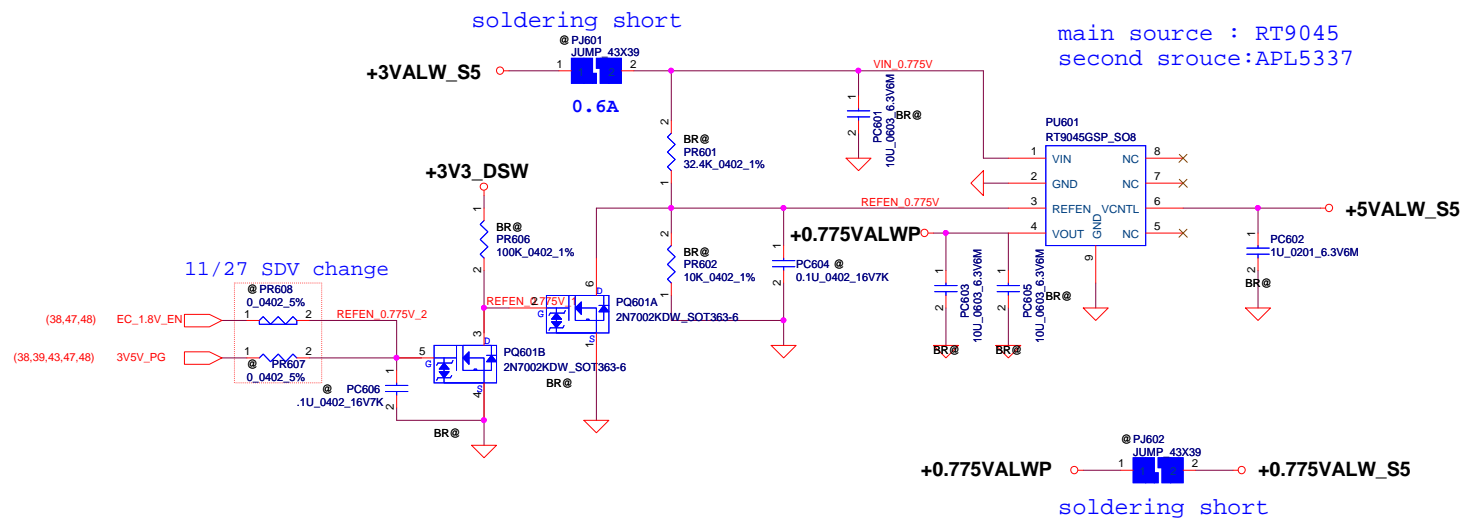
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+1.8VALWP
Ipeak=2A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.69A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.524A
LIR=Delta IL/Ipeak=0.26
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=18.3uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.65uF

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Vo	0.775	V
Vin	3.3	V
Io	0.2	A
PD	0.512	W
θJA(main)	39.8	°C/W
θJA(2nd)	55	°C/W

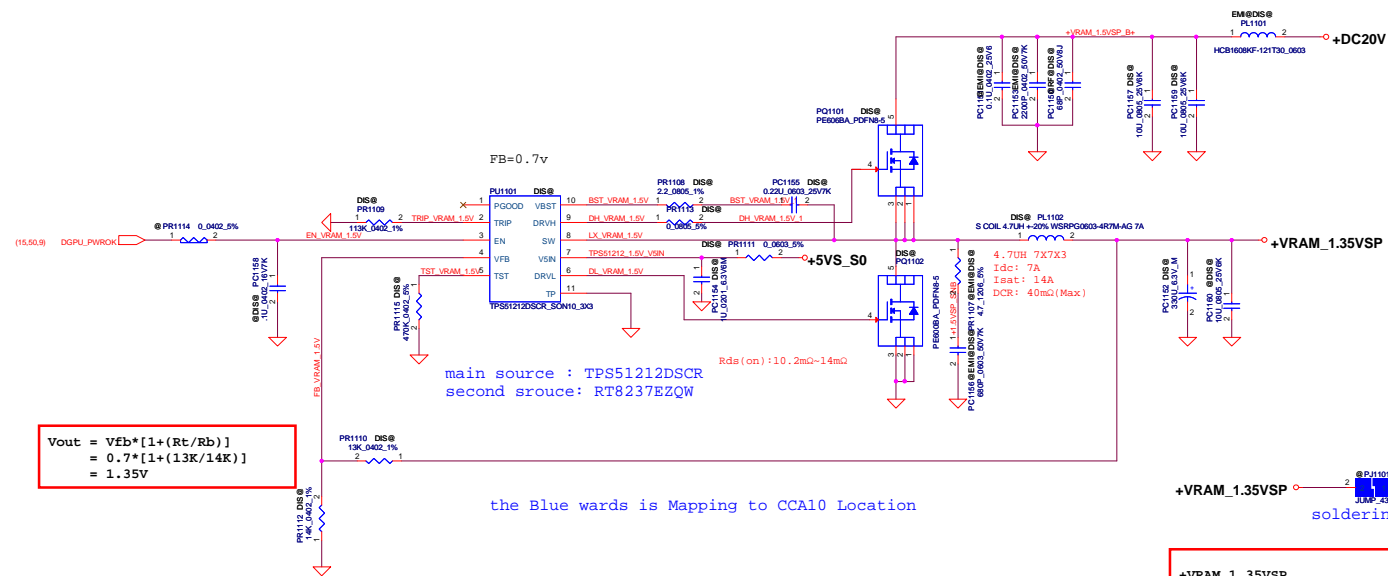
$$V_{out} = V_{in} \cdot R_2 / (R_1 + R_2)$$

$$= 3.3 \cdot [10K / 42.4K]$$

$$= 0.7783V$$

+0.775VS
Imax=0.2A ;

RT9045:
Current Limit=1.8A(min)~3.5A(Max)
PD = (VIN - VOUT) x IOUT + VIN x IQ
PD(MAX)=(3.3-0.775)*0.2+3.3*2.5mA = 0.5132W
θ JA= 39.8°C/W
IQ+2.5mA
PD*θJA = 20.425°C

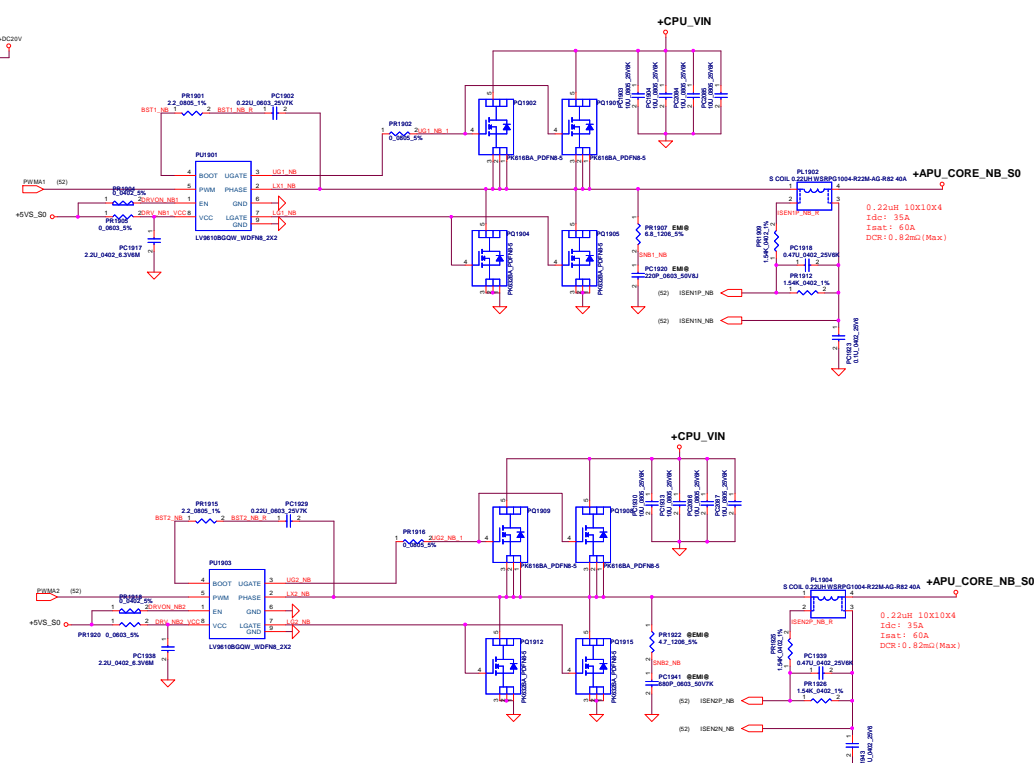
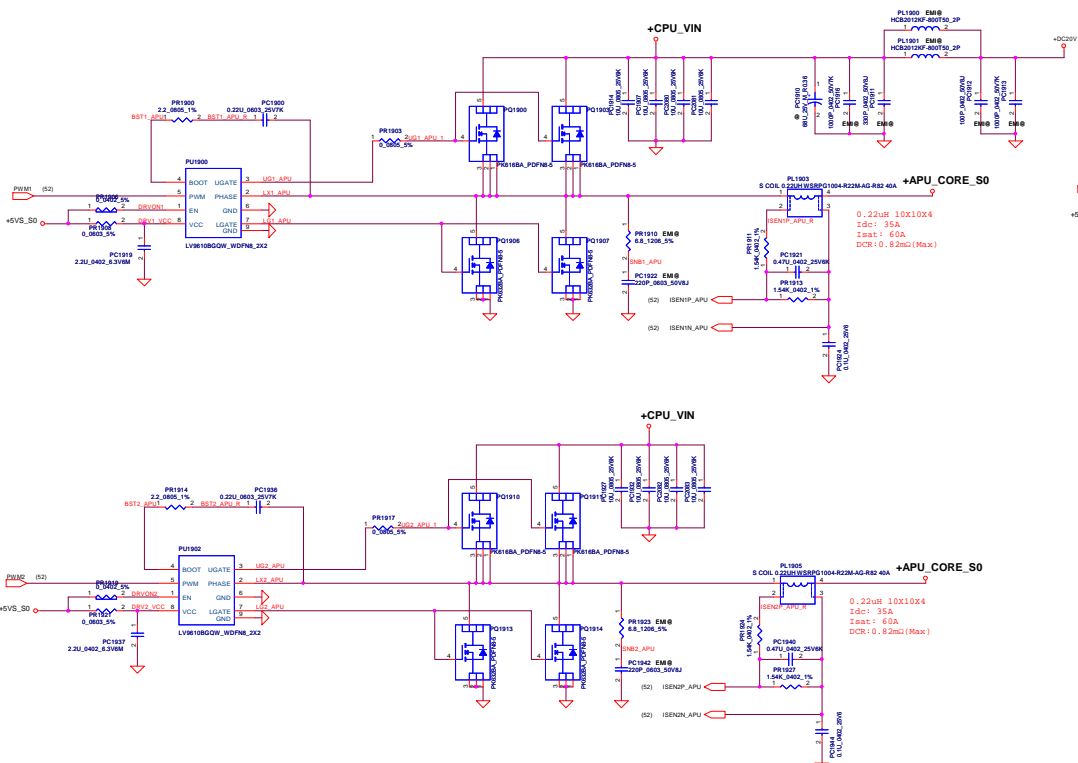


$$\begin{aligned} &+VRAM_1.35VSP \\ &V_{in} = 20V \\ &I_{in} = 1.35 \times 3.8 / 0.85 / 20 \\ &= 0.3A \end{aligned}$$

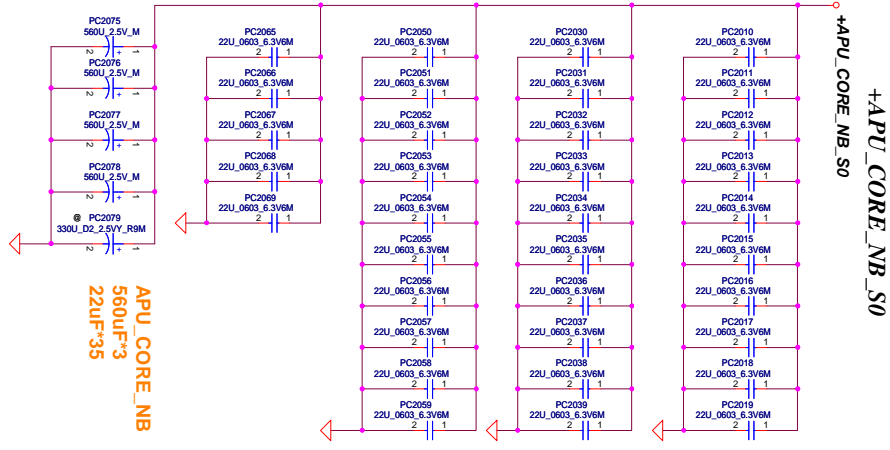
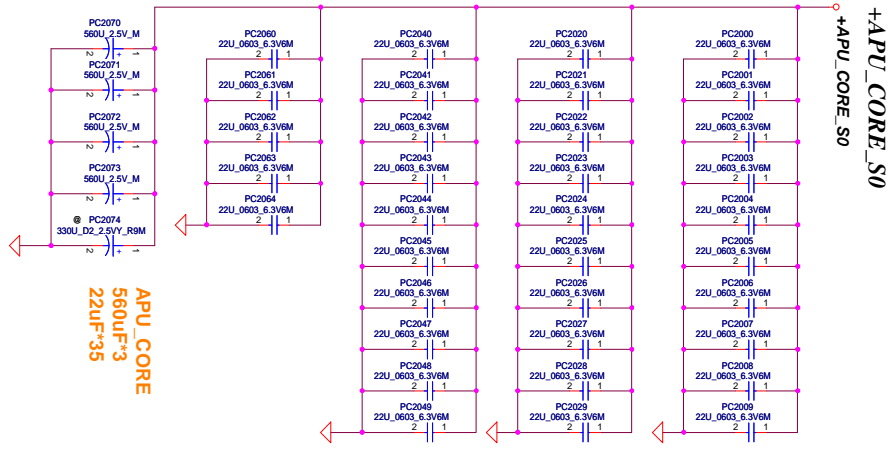
$$\begin{aligned} V_{out} &= V_{Eb} \times [1 + (R_t / R_b)] \\ &= 0.7 \times [1 + (13K / 14K)] \\ &= 1.35V \end{aligned}$$

$$\begin{aligned} &+VRAM_1.35VSP \\ &I_{max} = 2.66A, I_{peak} = 3.8A ; f_{sw} = 300KHz \\ &I_{ocp} = (R_{cs1} \times I_{trip}) / R_{ds(on)} \\ &R_{ds} : L/S \rightarrow typ: 10.2m\Omega ; max: 14m\Omega \\ &I_{trip} = 9-11 \mu A \\ &I_{ocp(set)} = 10.245-12.419A \\ &I_{in_ripple} = 0.566A \\ &Output\ Cap. ESR = 17m\Omega \\ &\Delta IL = [(V_{in} - V_o) / L] \times [(V_{out} / V_{in}) \times T] = 0.294A \\ &LIR = \Delta IL / I_{peak} = 0.243 \\ &C_{out} = [L \times (I_{out} + \Delta IL / 2)^2] / [(V_{out} + \Delta V)^2 - V_{out}^2] \\ &= 245\mu F \\ &CINBULK = I_{Load} \times V_{out} \times (V_{in} - V_{out}) / (f_{sw} \times V_{in}^2 \times VINPP) = 0.28\mu F \end{aligned}$$

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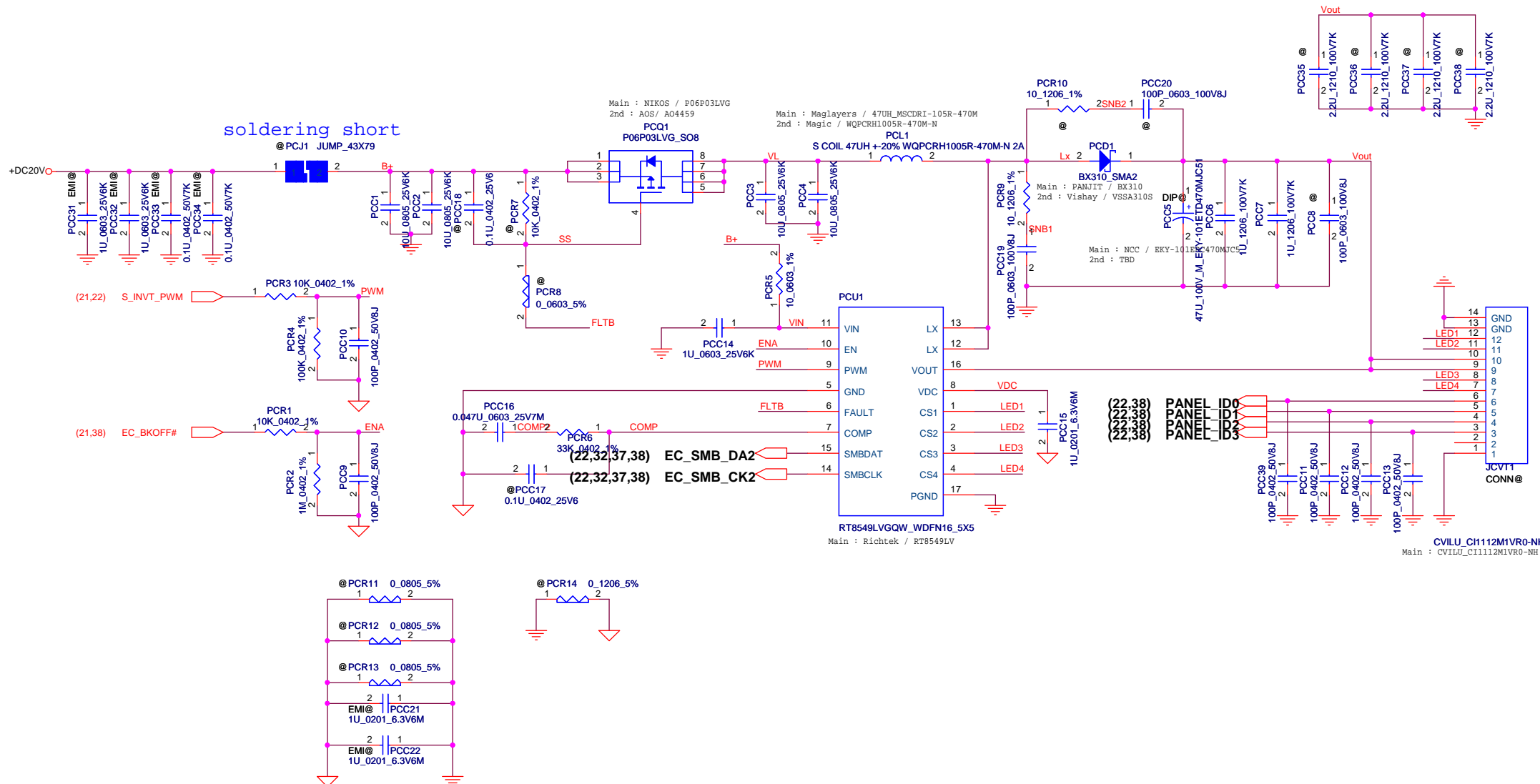
+APU_CORE_S0 TDC=39A, Ipeak=55A Fsw=400K, OCP>=83A Inductor DCR=0.82mohm Output Cap. ESR=10mohm Rds H/S --> typ: 4.8mohm ; max: 7mohm L/S --> typ: 2.1mohm ; max: 3.3mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.392 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =4136uF CINBULK=Iload*Vout*(Vin-Vout)/((Fsw*Vin^2*VINPP)=2.29uF	+APU_CORE_NB_S0 TDC=40A, Ipeak=60A Fsw=400K, OCP>=90A Inductor DCR=0.98mohm Output Cap. ESR=10mohm Rds H/S --> typ: 4.8mohm ; max: 7mohm L/S --> typ: 2.1mohm ; max: 3.3mohm Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.795A LIR=Delta IL/Ipeak=0.38 Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =4821uF CINBULK=Iload*Vout*(Vin-Vout)/((Fsw*Vin^2*VINPP)=2.49uF
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This is GND_POWER

soldering short



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				Date:	Sheet 55 of 58

